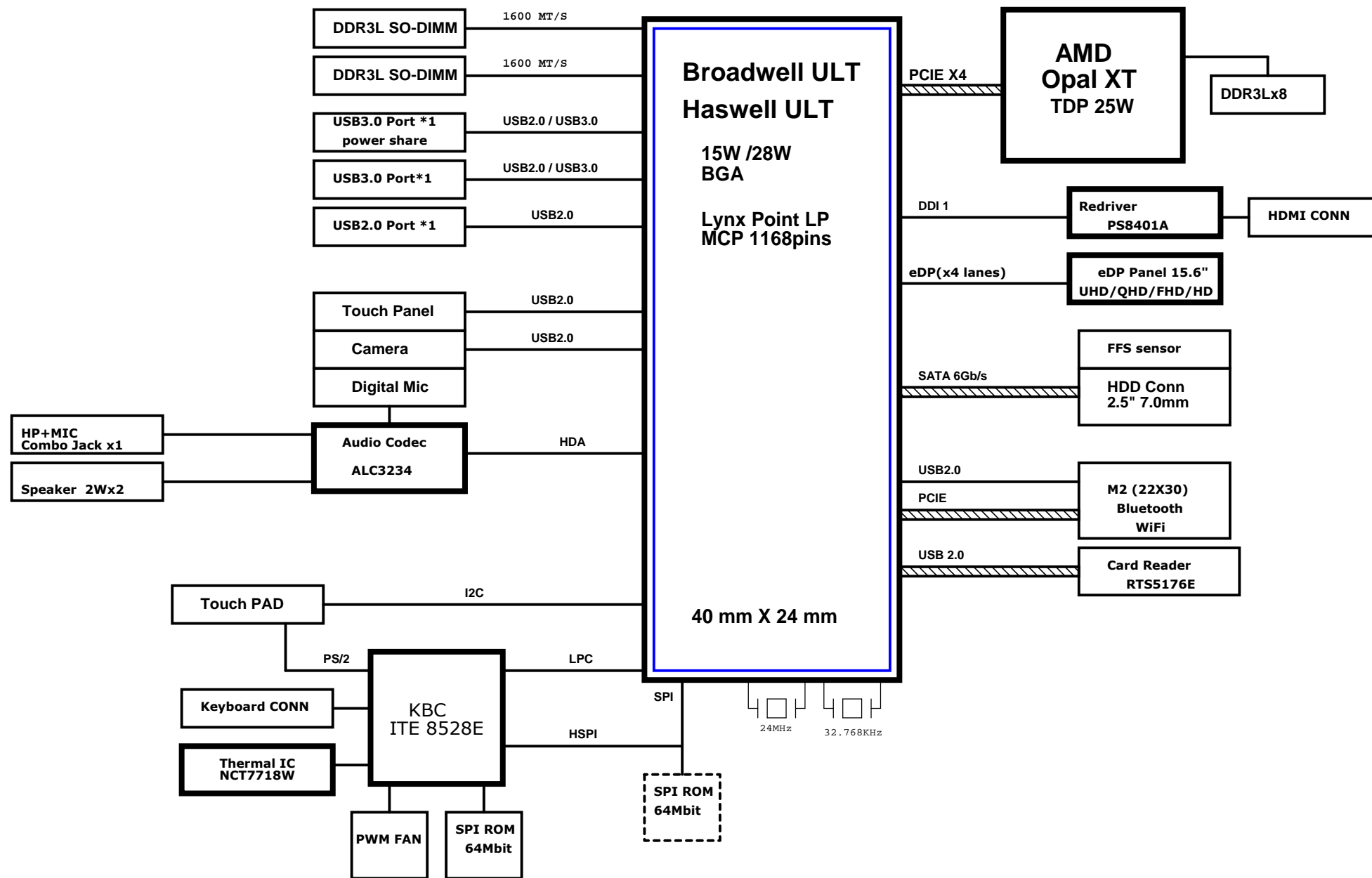


AM6 BLOCK DIAGRAM



Port	USB3.0	PCIE	SATA
1	USB3.0_1 Left Power Share		
2	USB3.0_2 Right		
3	USB3.0_3 X	PCIE1 X	
4	USB3.0_4 X	PCIE2 X	
5		PCIE3 X	
6		PCIE4 WIFI	
7		PCIE5 GPU 4X	
8		PCIE5 GPU 4X	
9		PCIE5 GPU 4X	
10		PCIE5 GPU 4X	
11		PCIE6 X	SATA3 X
12		PCIE6 X	SATA2 X
13		PCIE6 X	SATA1 HDD
14		PCIE6 X	SATA0 X

PCIE CLK
CLK0 X
CLK1 X
CLK2 X
CLK3 WIFI
CLK4 GPU 4X
CLK5 X

USB2.0
USB2.0_0 Left Power Share
USB2.0_1 Right /w 3.0
USB2.0_2 Right
USB2.0_3 Card Reader
USB2.0_4 Camera
USB2.0_5 eTP
USB2.0_6 Blue Tooth
USB2.0_7 X



Quanta Computer Inc.

PROJECT : AM6

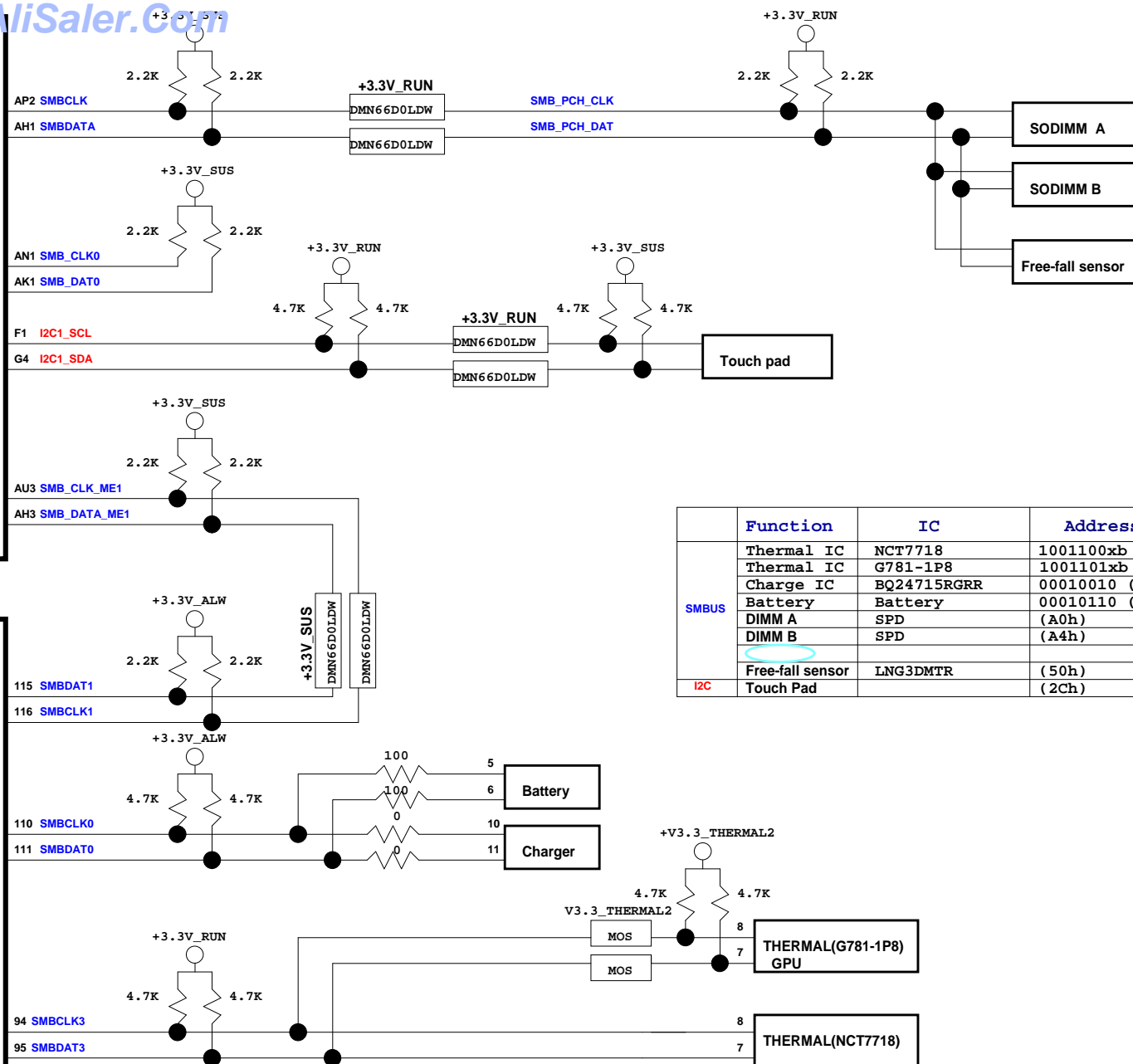
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PORT ASSIGNMENT

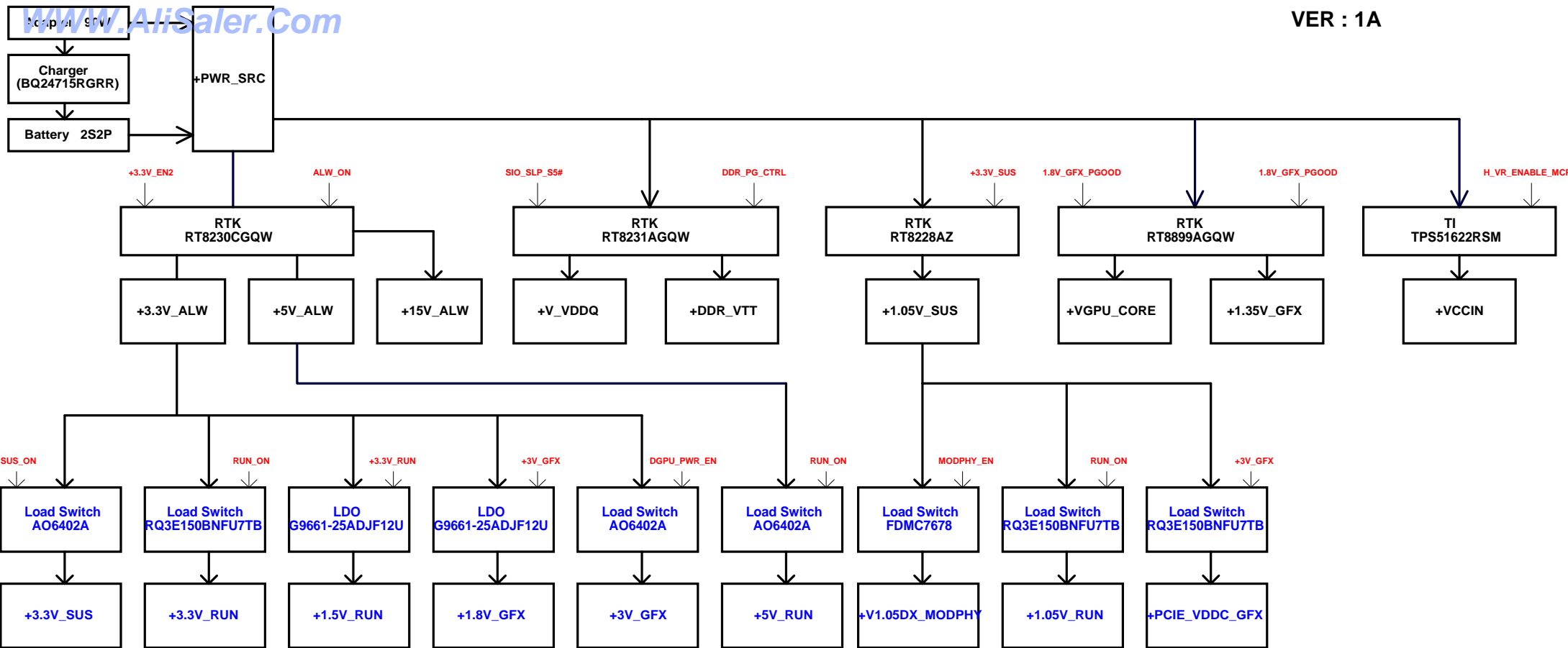
Haswell
ULT

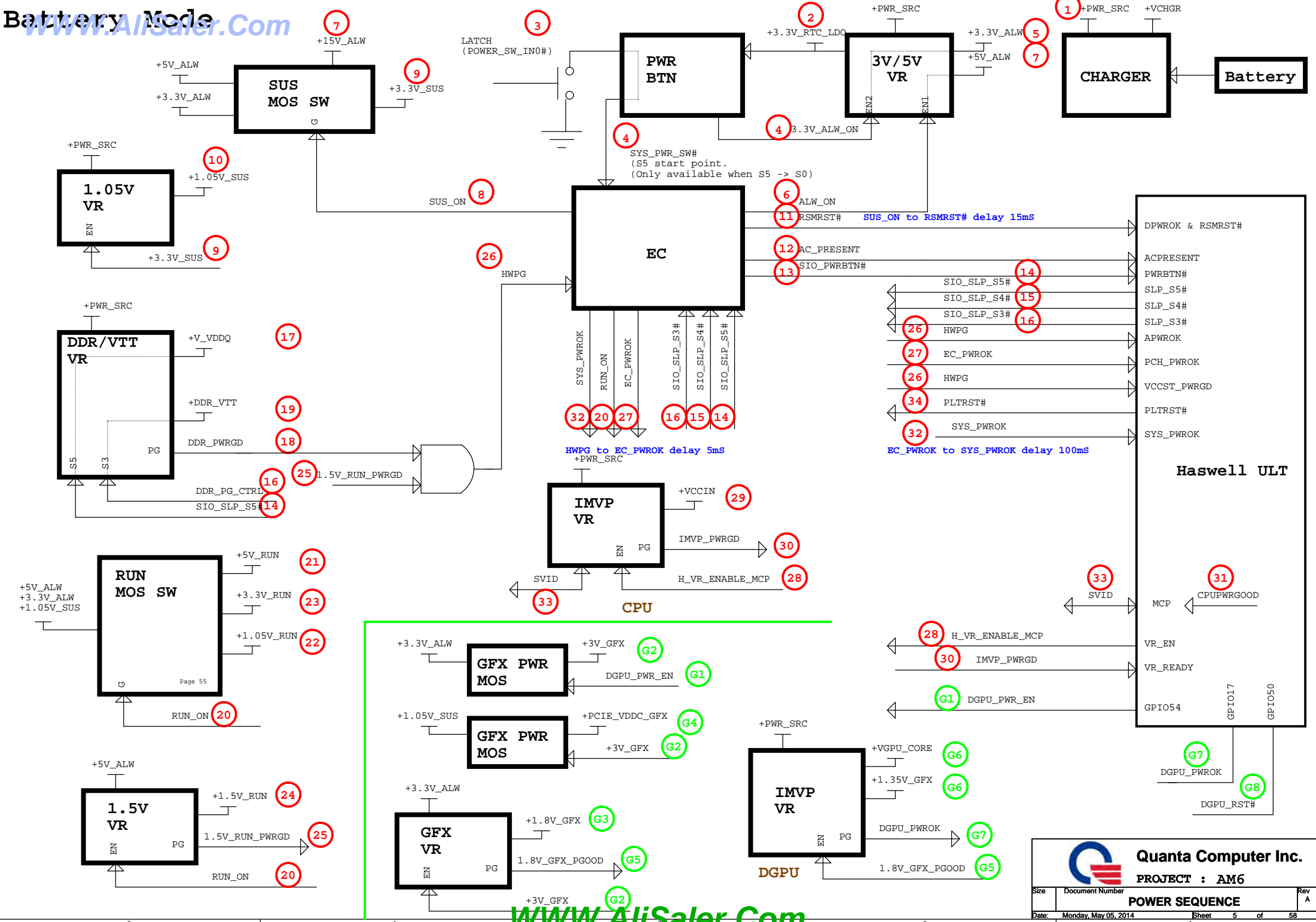
MB

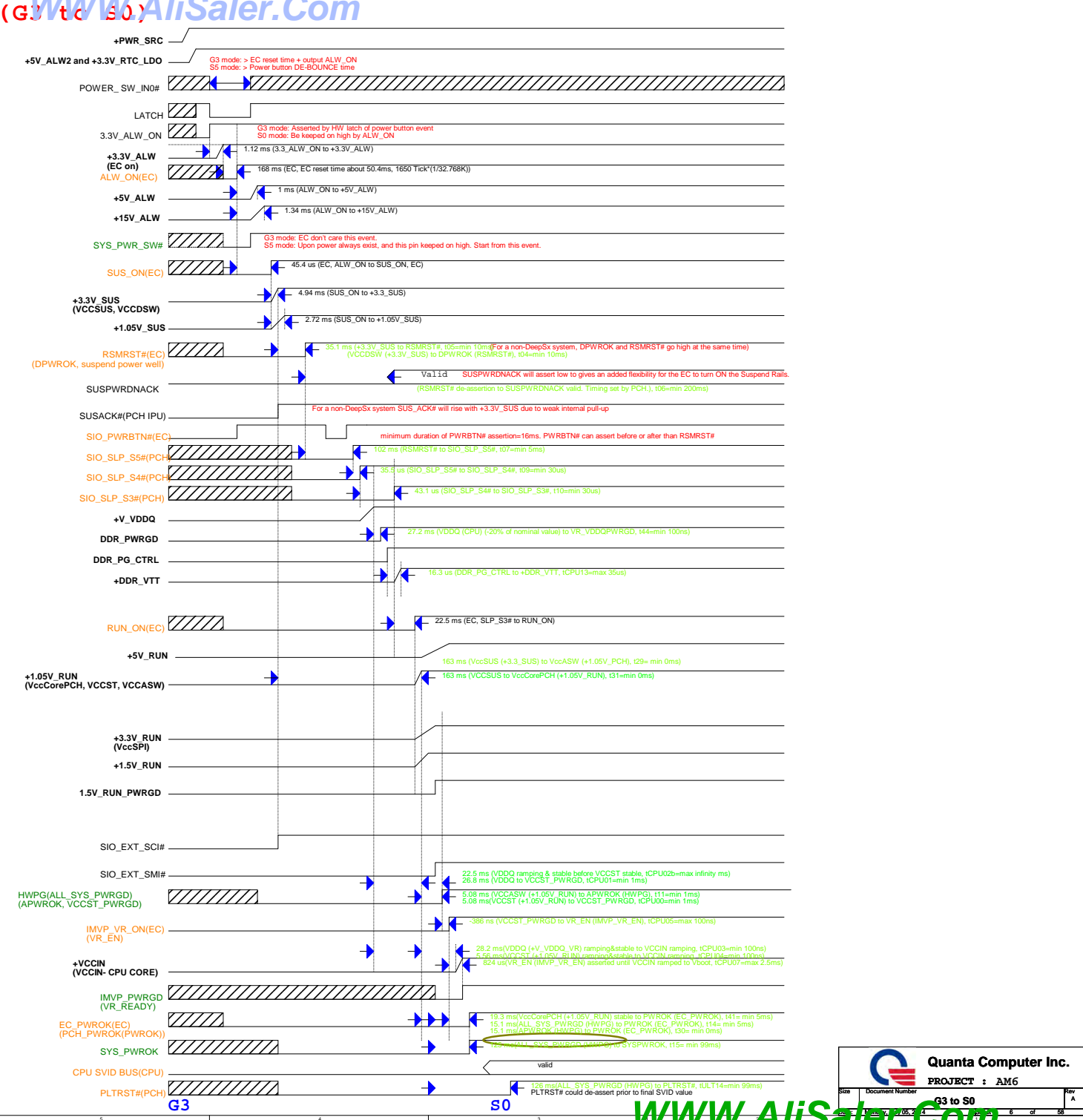
SIO
ITE8528E



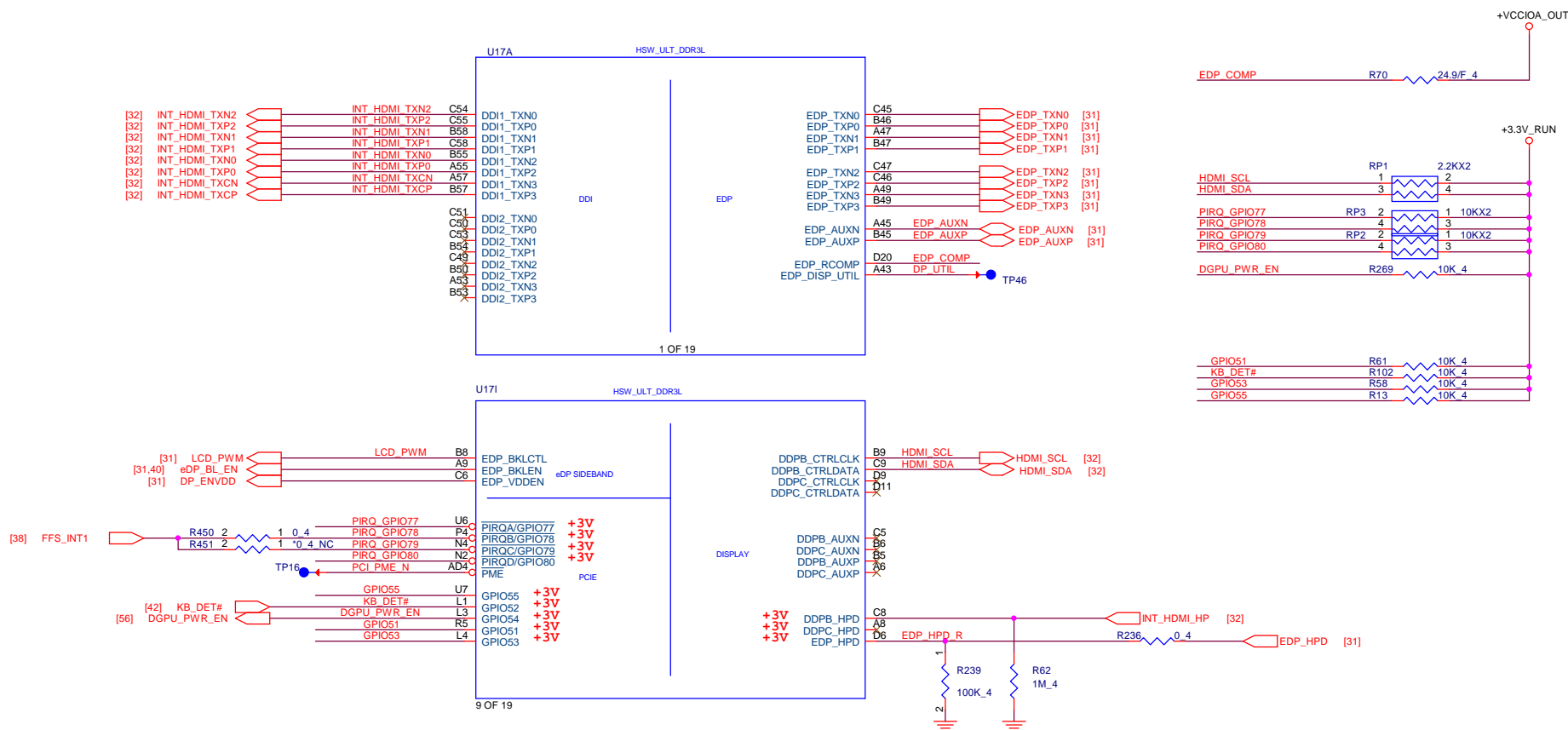
	Function	IC	Address
SMBUS	Thermal IC	NCT7718	1001100xb (98h)
	Thermal IC	G781-1P8	1001101xb (9Ah)
	Charge IC	BQ24715RGRR	00010010 (0x12h)
	Battery	Battery	00010110 (0X16h)
	DIMM A	SPD	(A0h)
	DIMM B	SPD	(A4h)
	Free-fall sensor	LNG3DMTR	(50h)
I2C	Touch Pad		(2Ch)







Haswell ULT (DISPLAY)

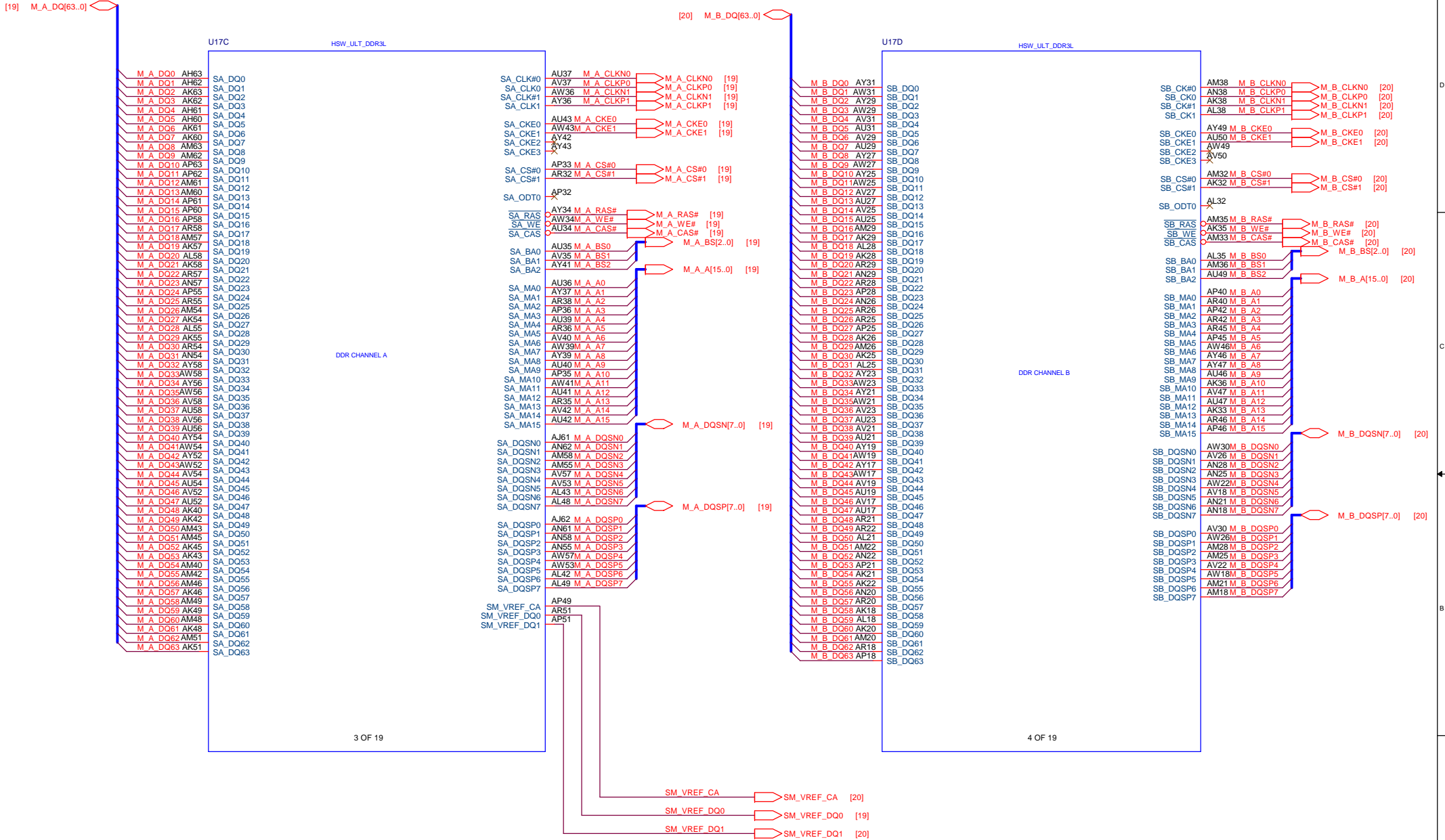


PCH Strap Table

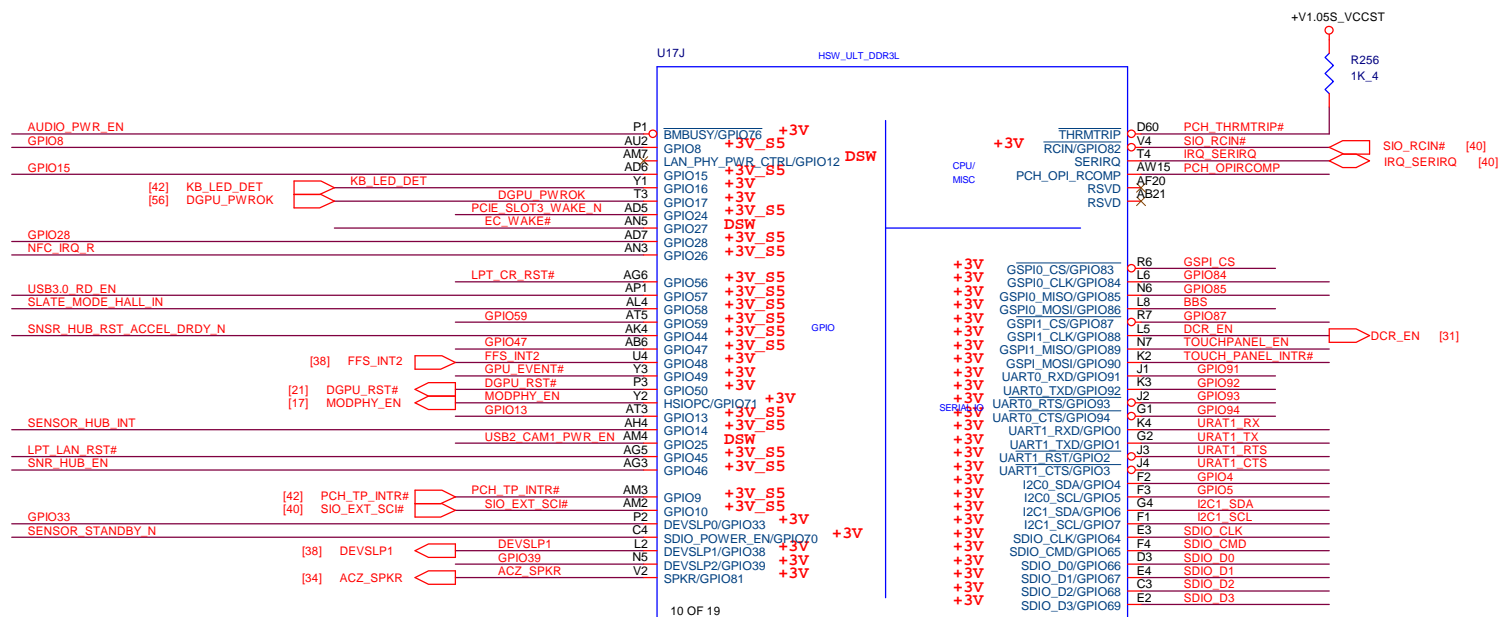
Pin Name	Strap description	Sampled	Configuration	note
DDPB_CTRLDATA	Port B Detected	PCH_PWROK	0 = Port B is not detected. 1 = Port B is detected.	This signal has a weak internal pull-down. IPD 20K is disabled when PLTRST# is de-asserted. PU 2.2K to +3.3V_RUN
DDPC_CTRLDATA	Port C Detected	PCH_PWROK	0 = Port C is not detected. 1 = Port C is detected.	This signal has a weak internal pull-down. IPD 20K is disabled when PLTRST# is de-asserted. NC



Haswell ULT (DDR3L)

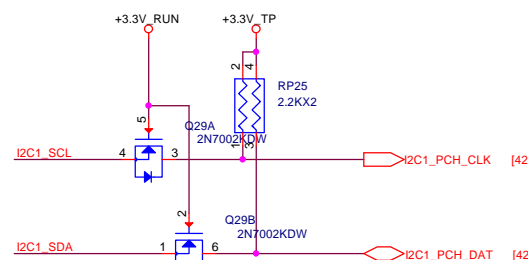
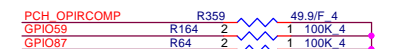
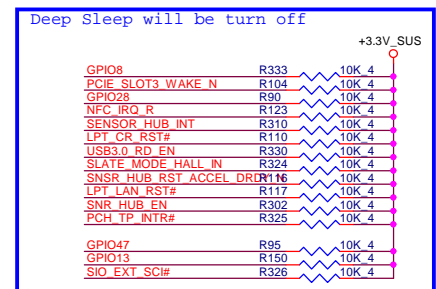
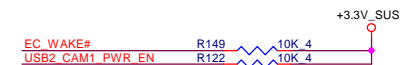
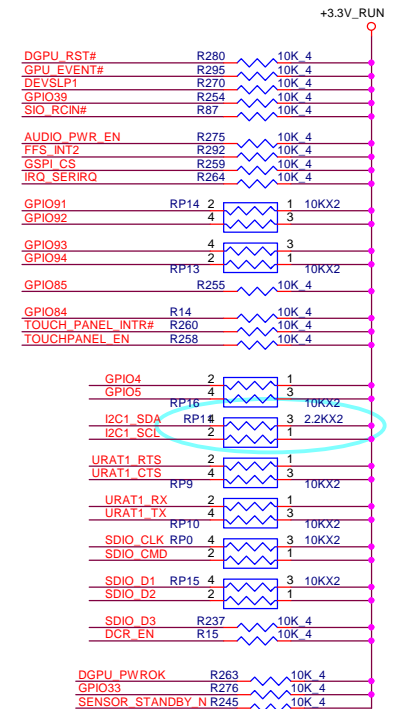


Hasswell ULT(GPIO,LPIO,MISC)

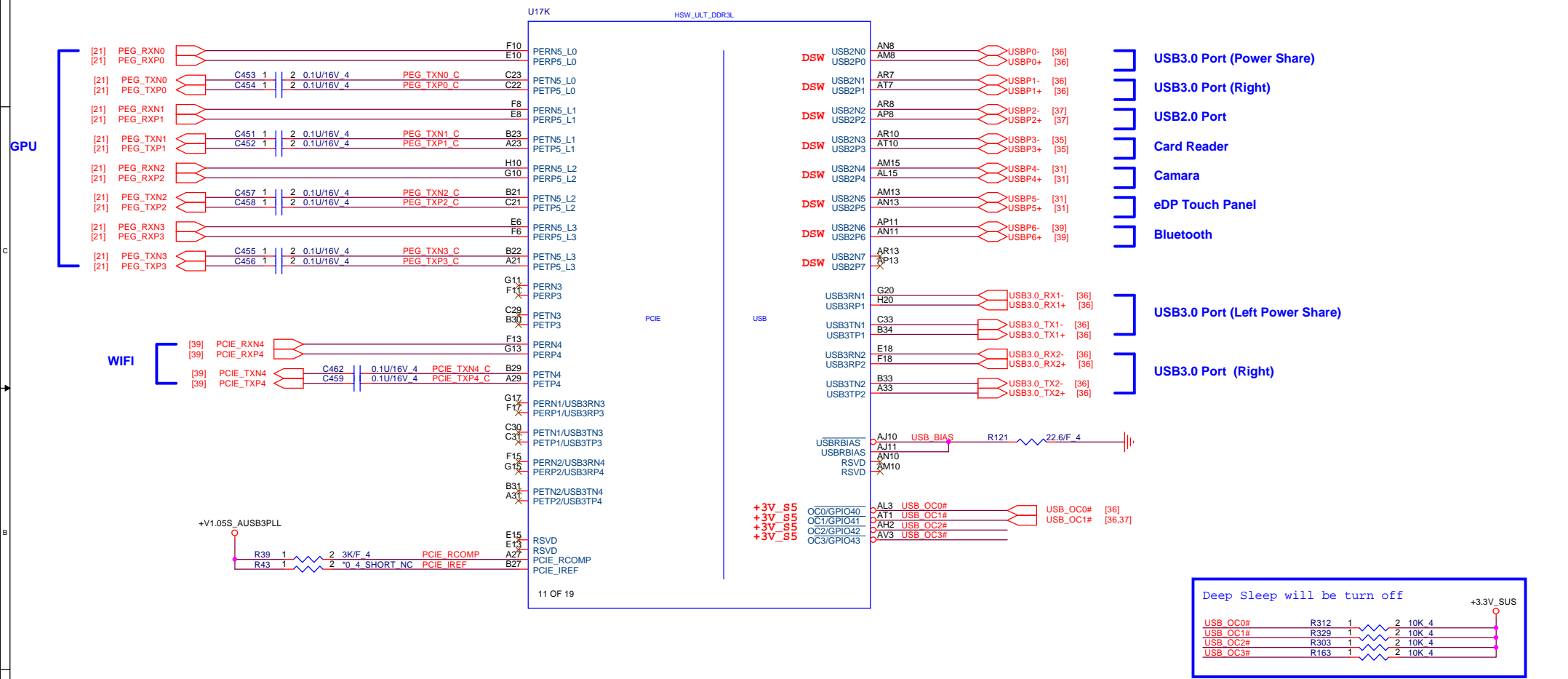


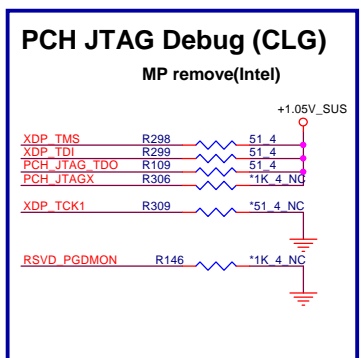
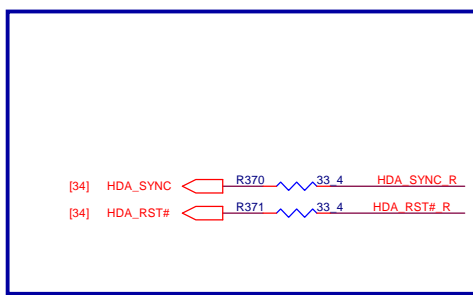
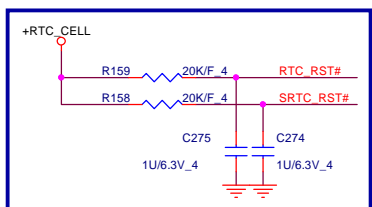
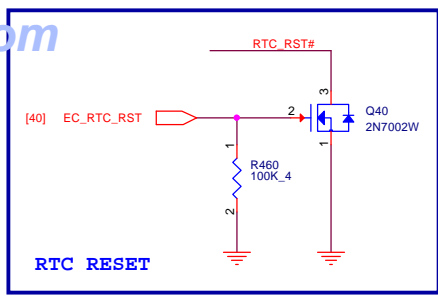
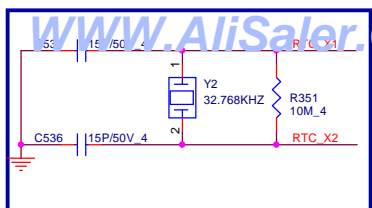
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
GPIO15	TLS Confidentiality	RSMRST#	<div>0 = Disable</div> <div>1 = Enable</div>	This signal has a weak internal pull-down. Deep Sleep will be turn off
SPKR/GPIO81	No Reboot mode	PCH_PWROK	<div>0 = Disable</div> <div>1 = Enable</div>	This signal has a weak internal pull-down. NA
GSPI0_MOSI/GPIO86	Boot BIOS Strap Bit (BBS)	PCH_PWROK	<div>0 = SPI</div> <div>1 = LPC</div>	This signal has a weak internal pull-down.
SDIO_D0/GPIO66	Top Swap Override	PCH_PWROK	<div>0 = Disable</div> <div>1 = Enable</div>	This signal has a weak internal pull-down.



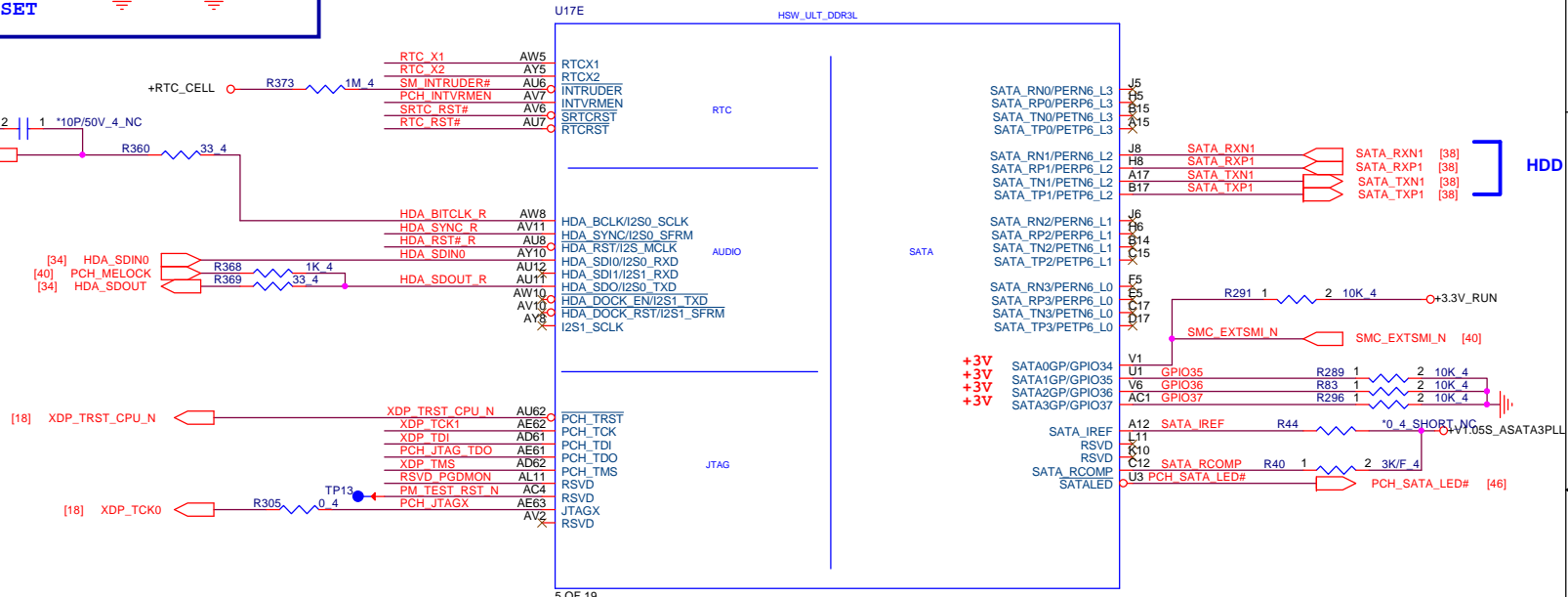
Haswell ULT (PCIE,USB)





DFXTESTMODE
HIGH - DFXTESTMODE DISABLED(DEFAULT)
LOW - DFXTESTMODE ENABLED

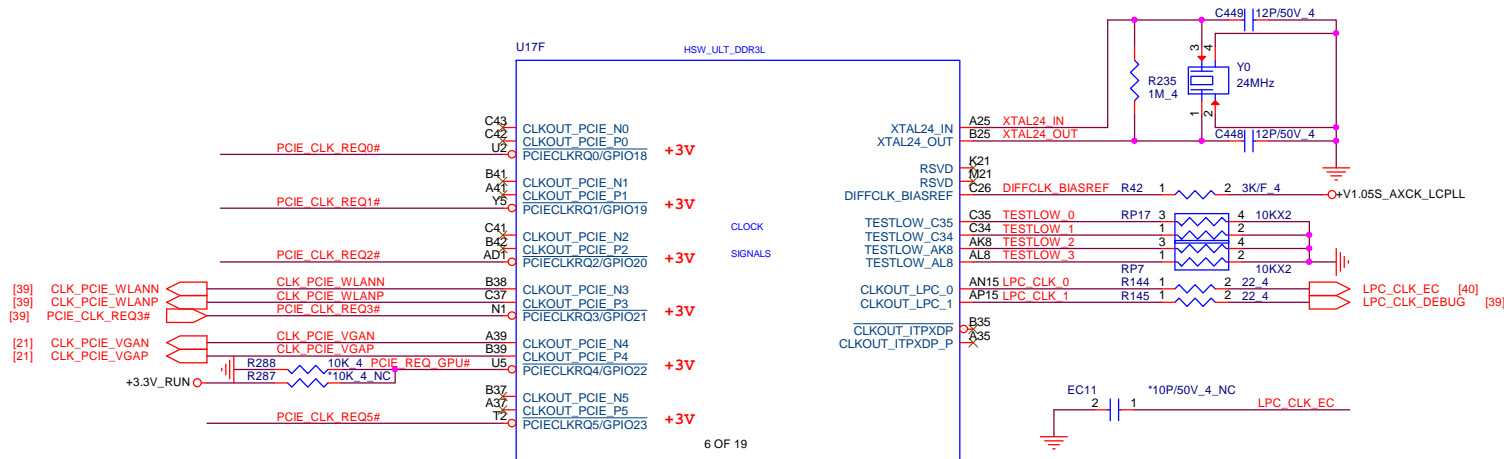
Haswell ULT (RTC, HDA, JTAG, SATA)



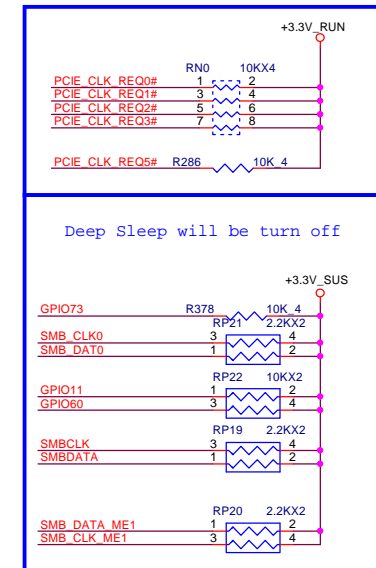
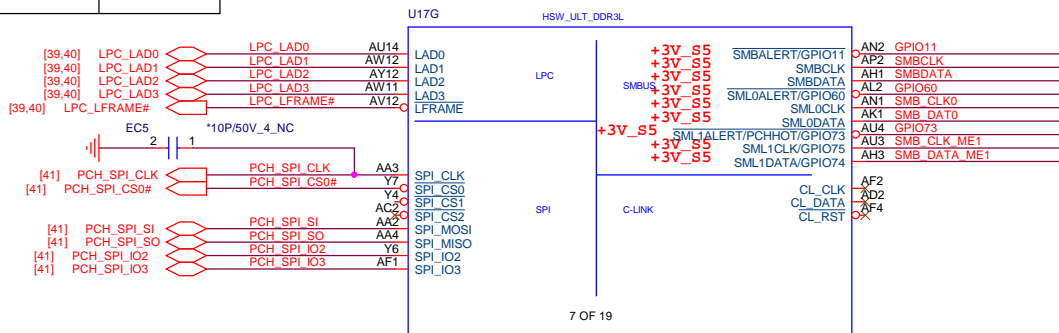
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = Security Effect (Int PD) 1 = Can be Override	This signal has a weak internal pull-down. The internal pull-down is disabled after PLTRST# deasserts
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	0 = Integrated VRMs disabled. 1 = Integrated VRMs enabled.	+RTC_CELL R157 330K 4 NC PCH_INTVRMEN R147 330K 4 An external resistor is required

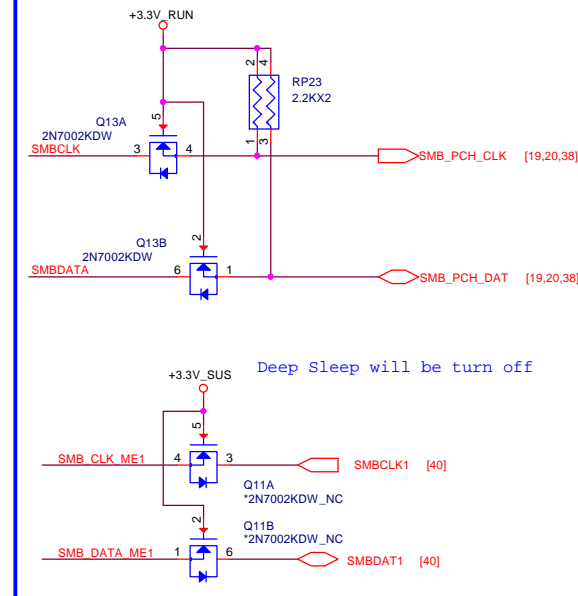
Haswell ULT (CLK)

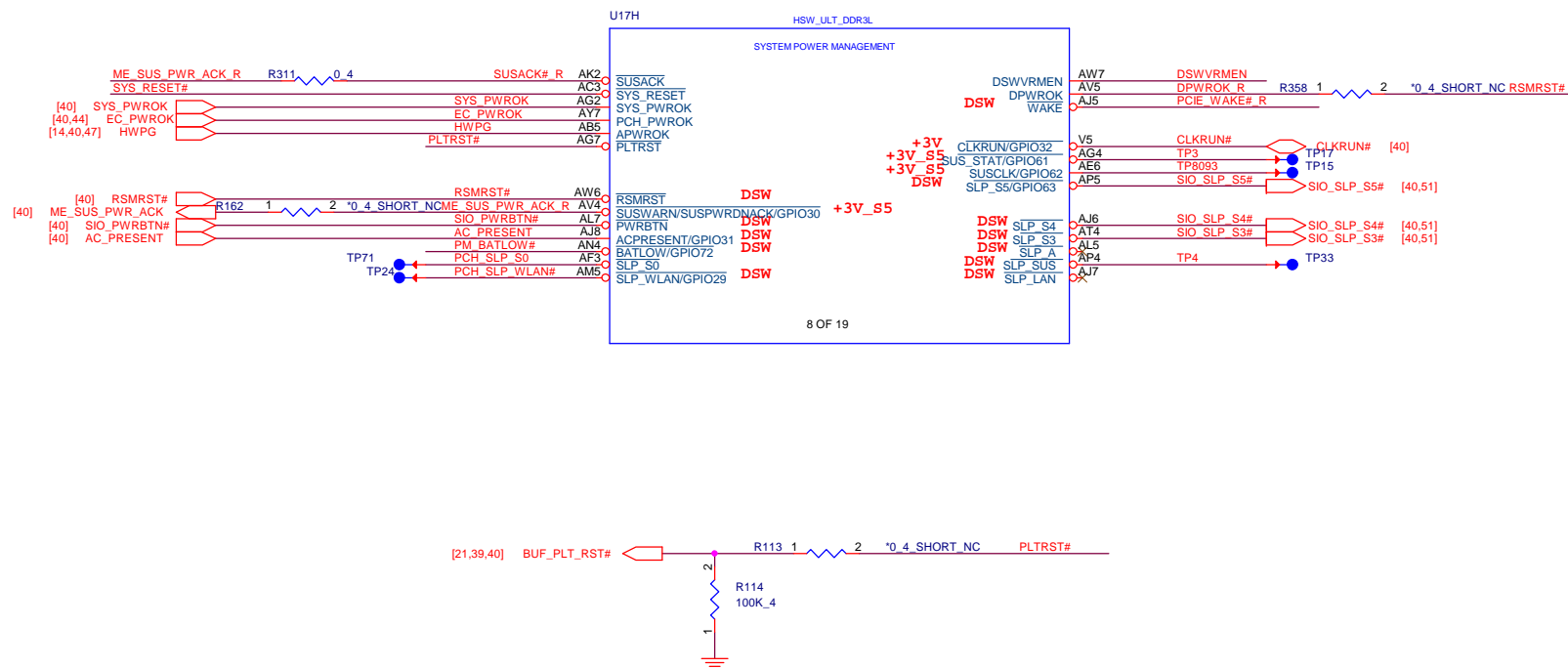


Haswell ULT (LPC/SPI/SMB/CLINK)

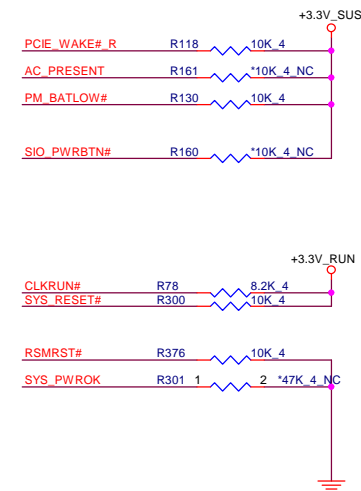


SMBus/Pull-up(CLG)

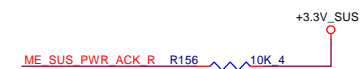





PCH Pull-high/low(CLG)



Deep Sleep will be turn off



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
DSWVRMEN	DeepSx Well On-Die Voltage Regulator Enable	ALWAYS	<div> <div>0 = Disable</div> <div>1 = Enable</div> </div>	1. This signal is always sampled. 2. This signal is in the RTC well. 

Haswell ULT MCP (POWER)

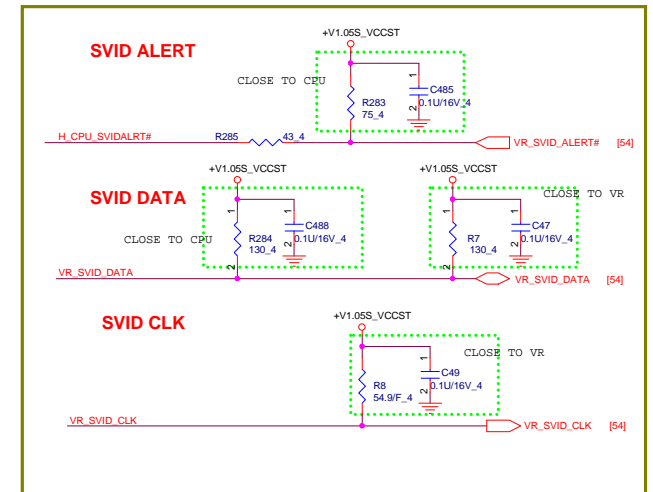
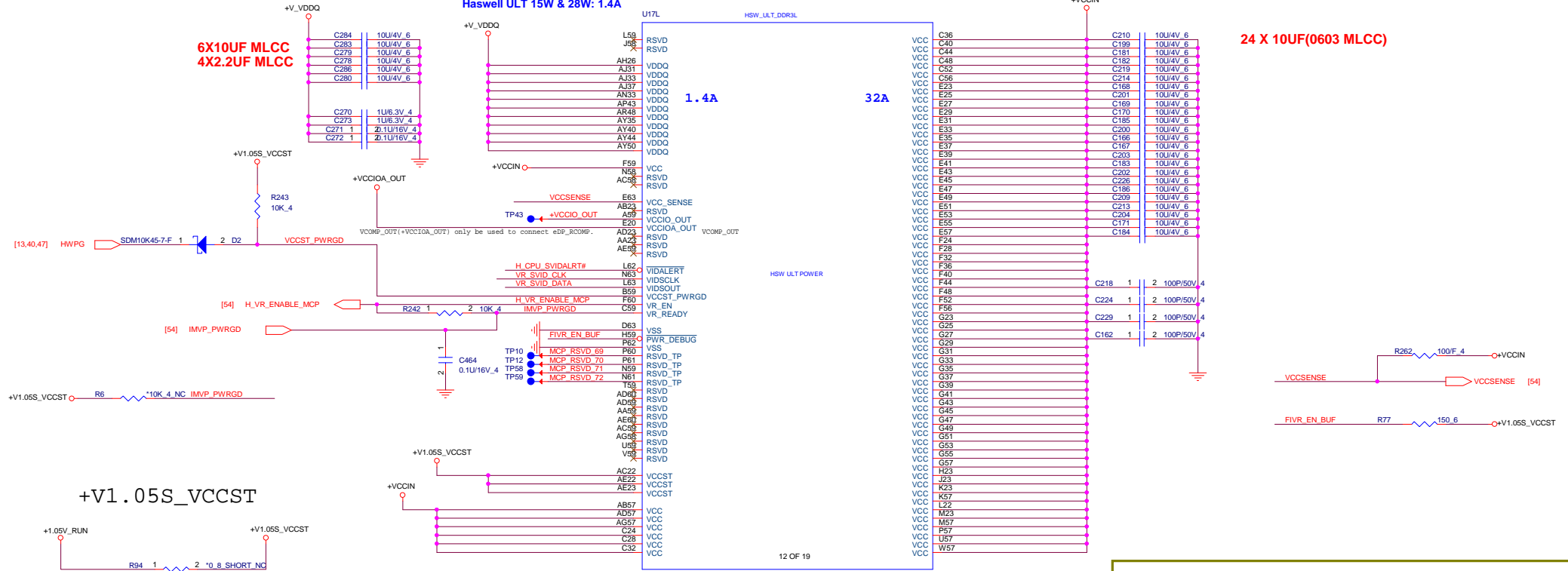
CPU VDDQ
Haswell ULT 15W & 28W: 1.4A

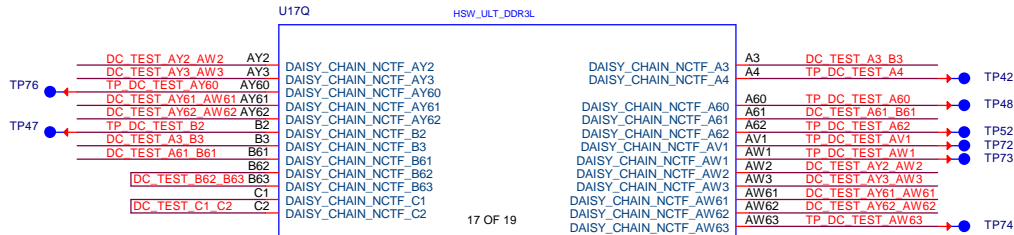
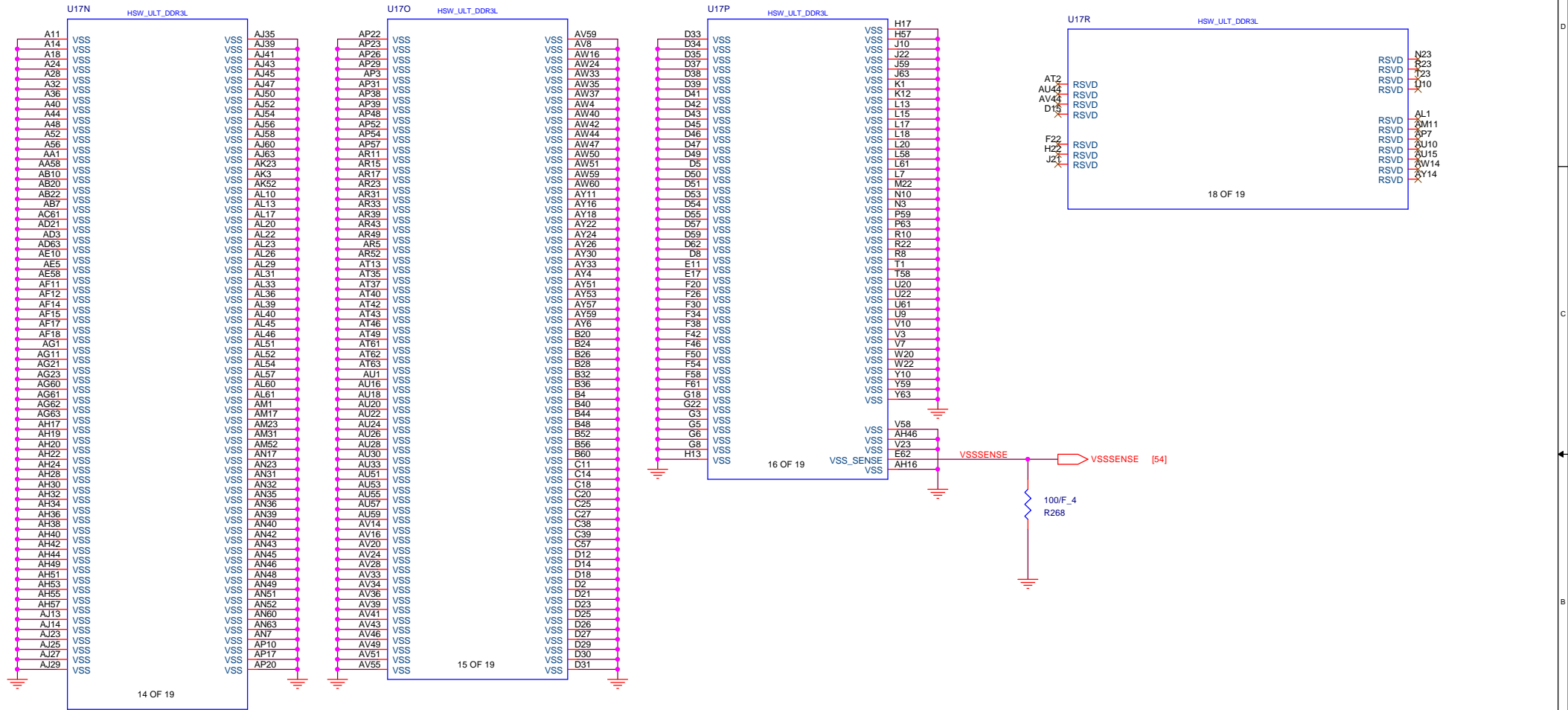
CPU VCC

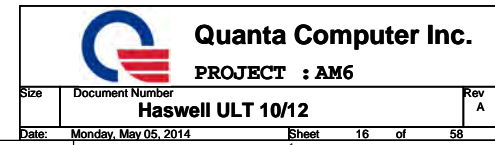
Haswell ULT 15W : 32A
28W : 40A

6X10UF MLCC
4X2.2UF MLCC

24 X 10UF(0603 MLCC)



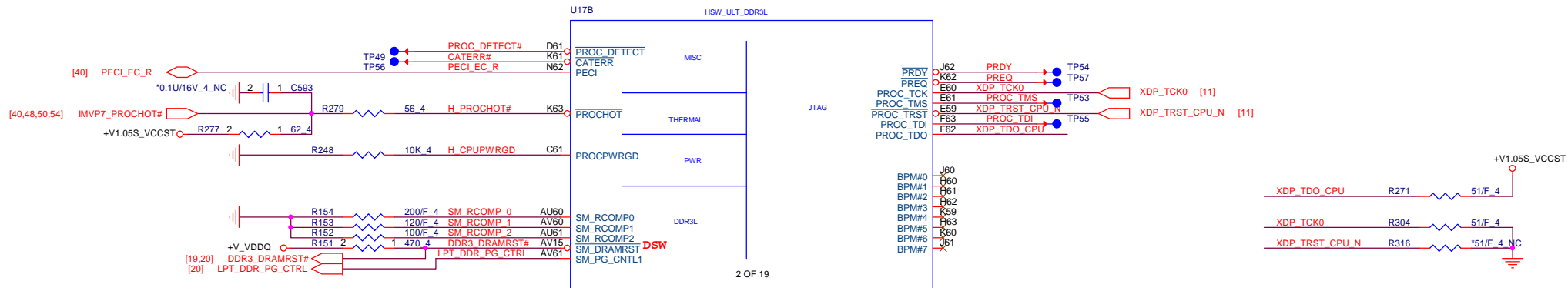




The CFG signals have a default value of '1' if not terminated on the board.

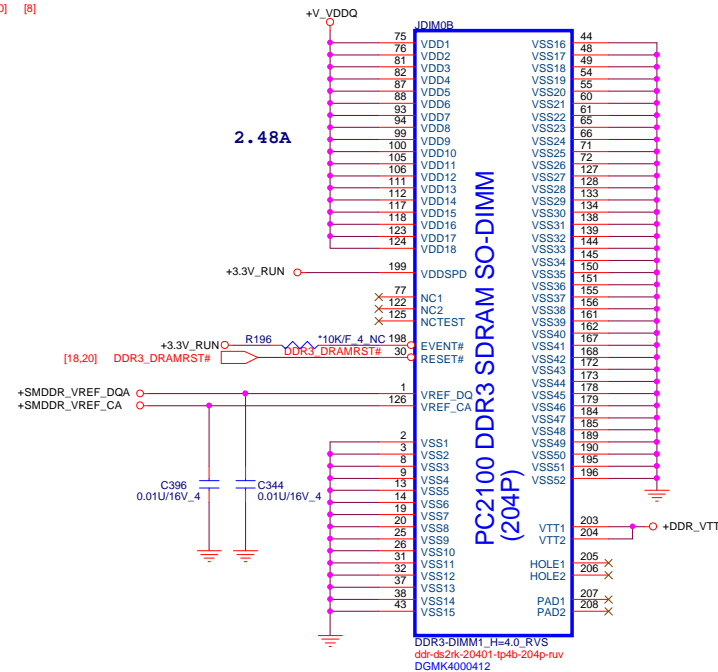
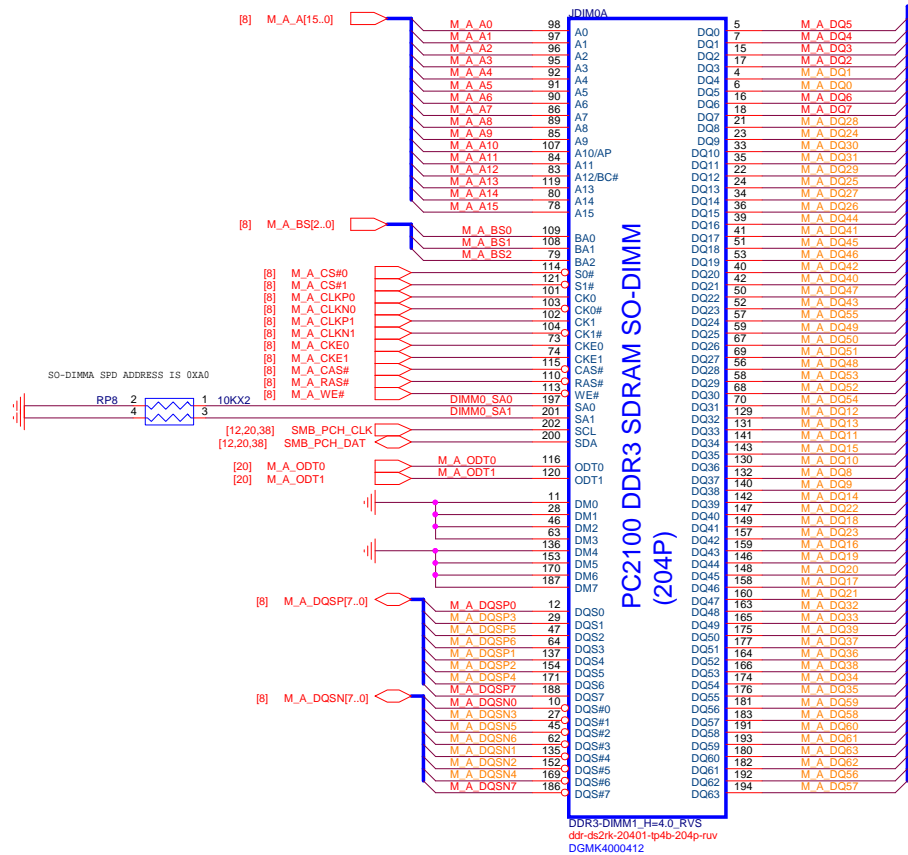
	1	0	
CFG0 Reserved	(DEFAULT) NORMAL OPERATION		
CFG1 Reserved	(DEFAULT) NORMAL OPERATION		
CFG2 Reserved	(DEFAULT) NORMAL OPERATION		
CFG3 MSR Privacy Bit Feature	Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting	IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden	
CFG4 eDP enable	Disabled	Enabled	
CFG[19:5] Reserved	(DEFAULT) NORMAL OPERATION		



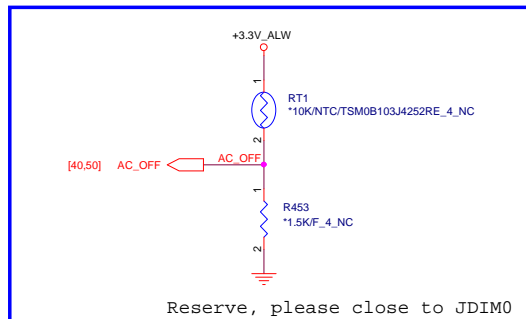
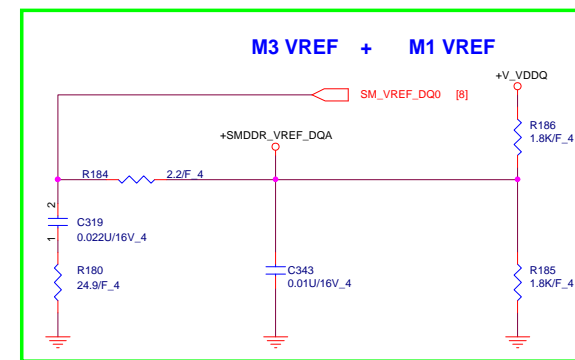
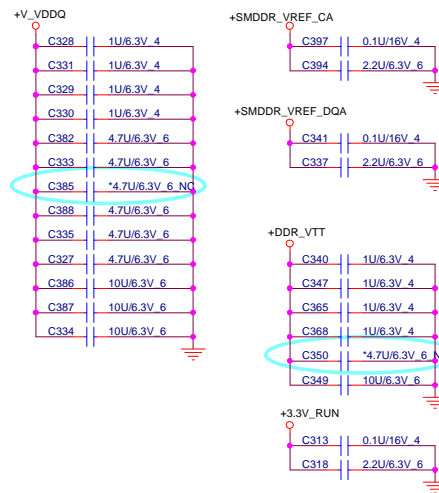


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Place these Caps near So-Dimm1.



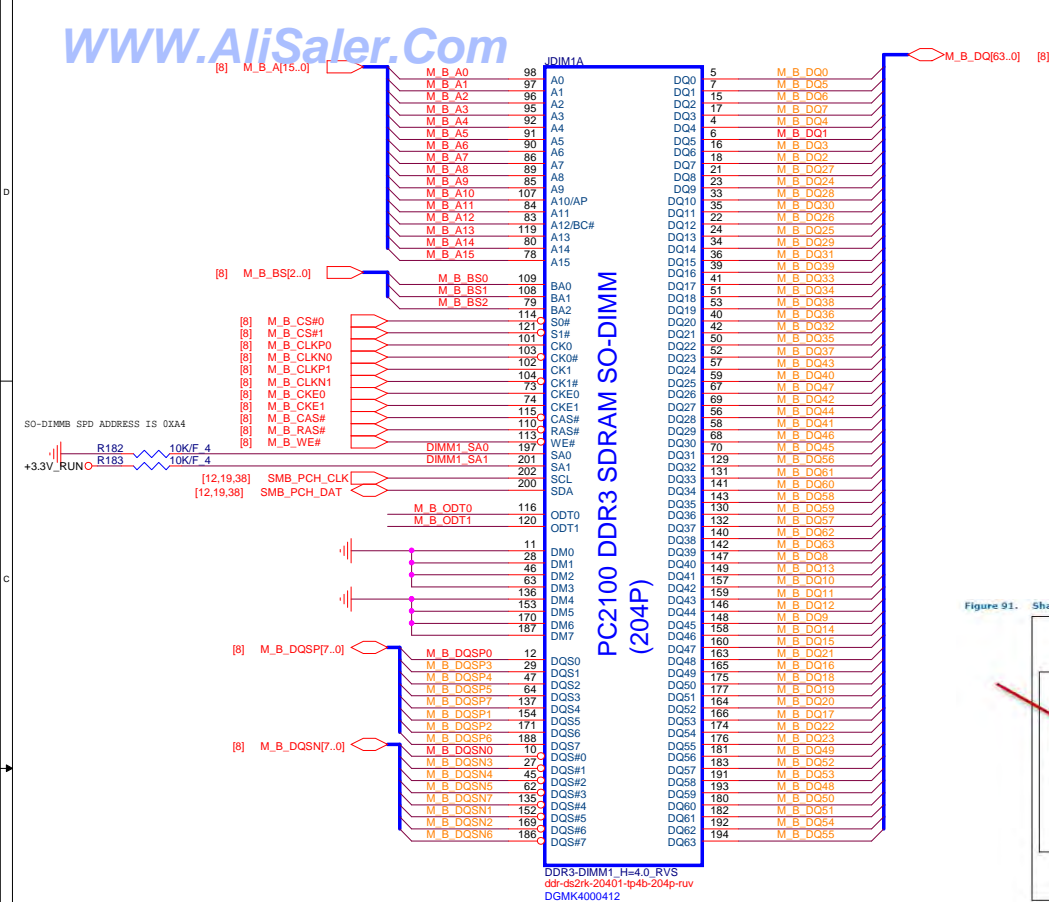
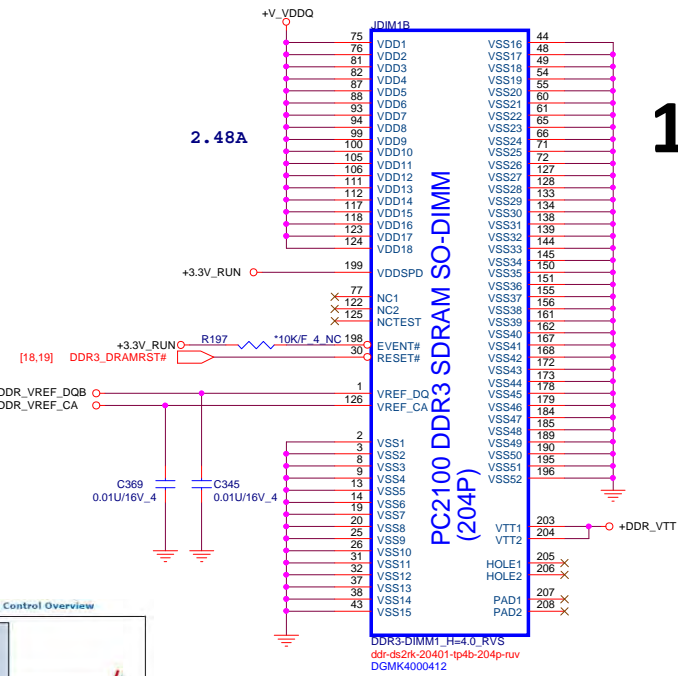
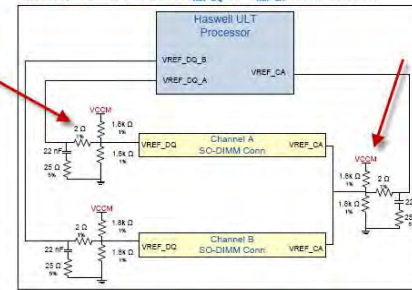
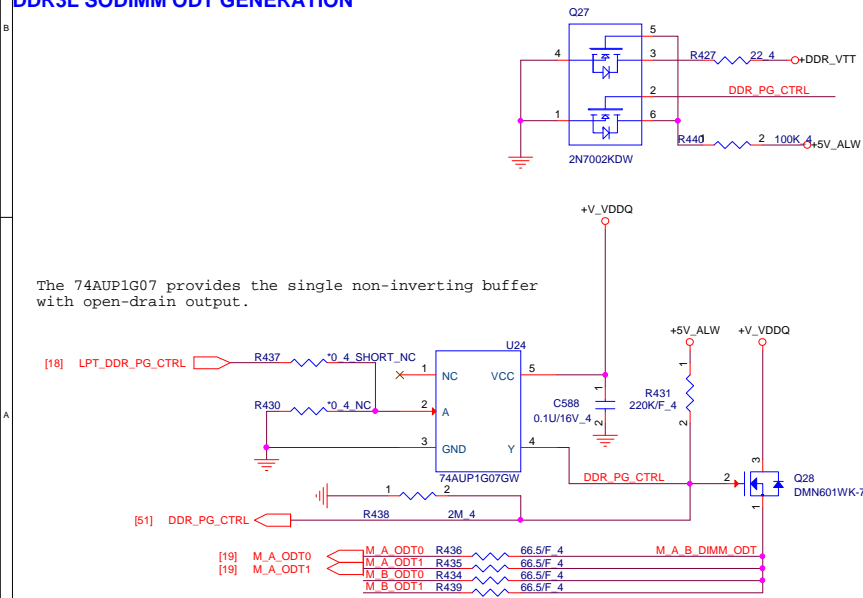


Figure 91. Shark Bay ULT DDR3L SODiMM V_{REF-DQ} and V_{REF-CA} Control Overview



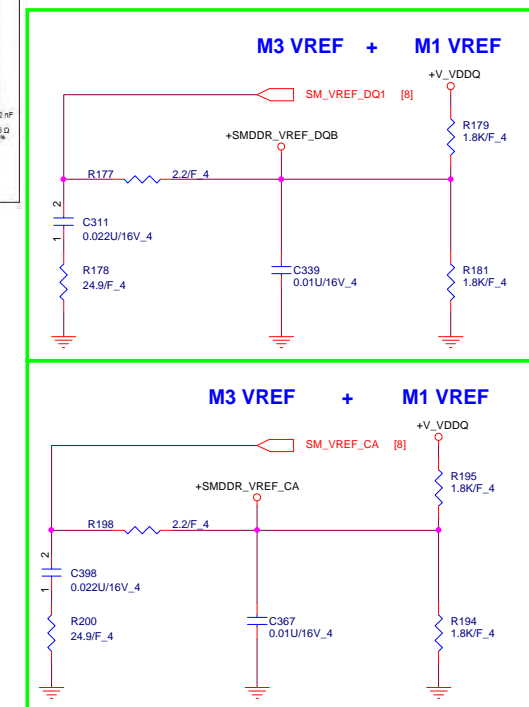
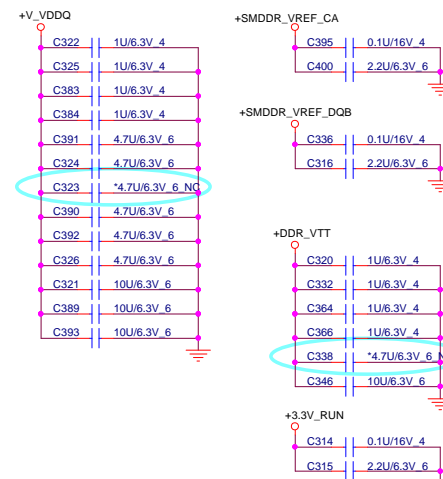
18

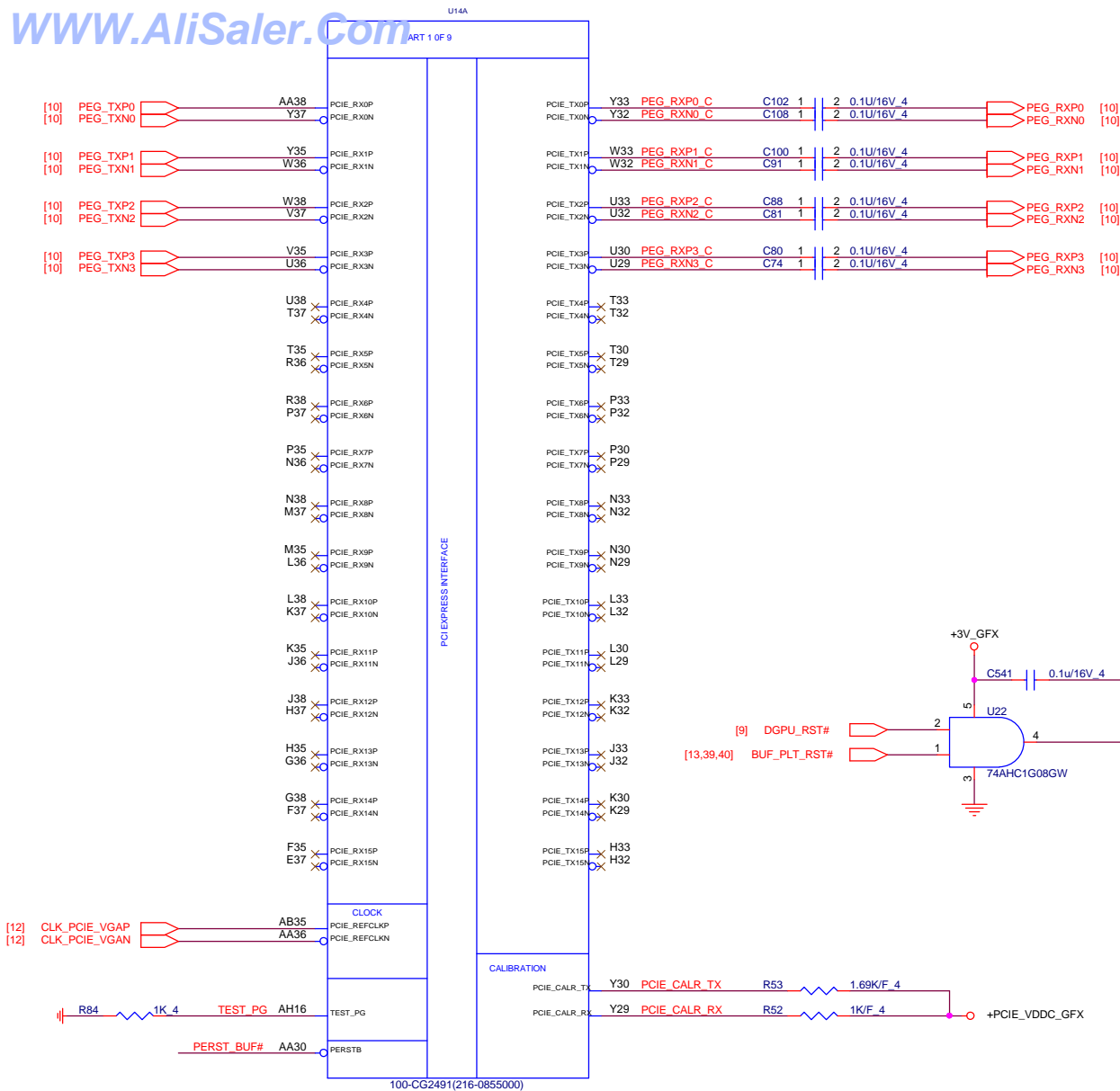
DDR3L SODIMM ODT GENERATION



The 74AUP1G07 provides the single non-inverting buffer with open-drain output.

Place these Caps near So-Dimm2.





Opal XT Power-on sequence

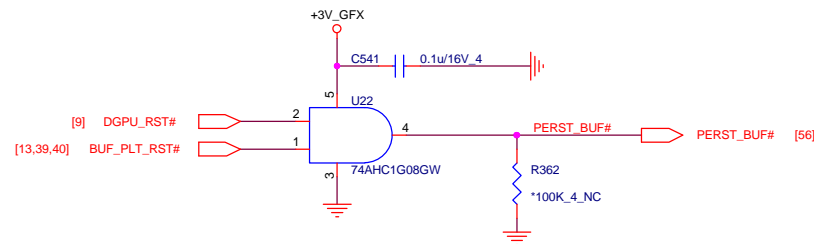
DGPU_PWR_EN

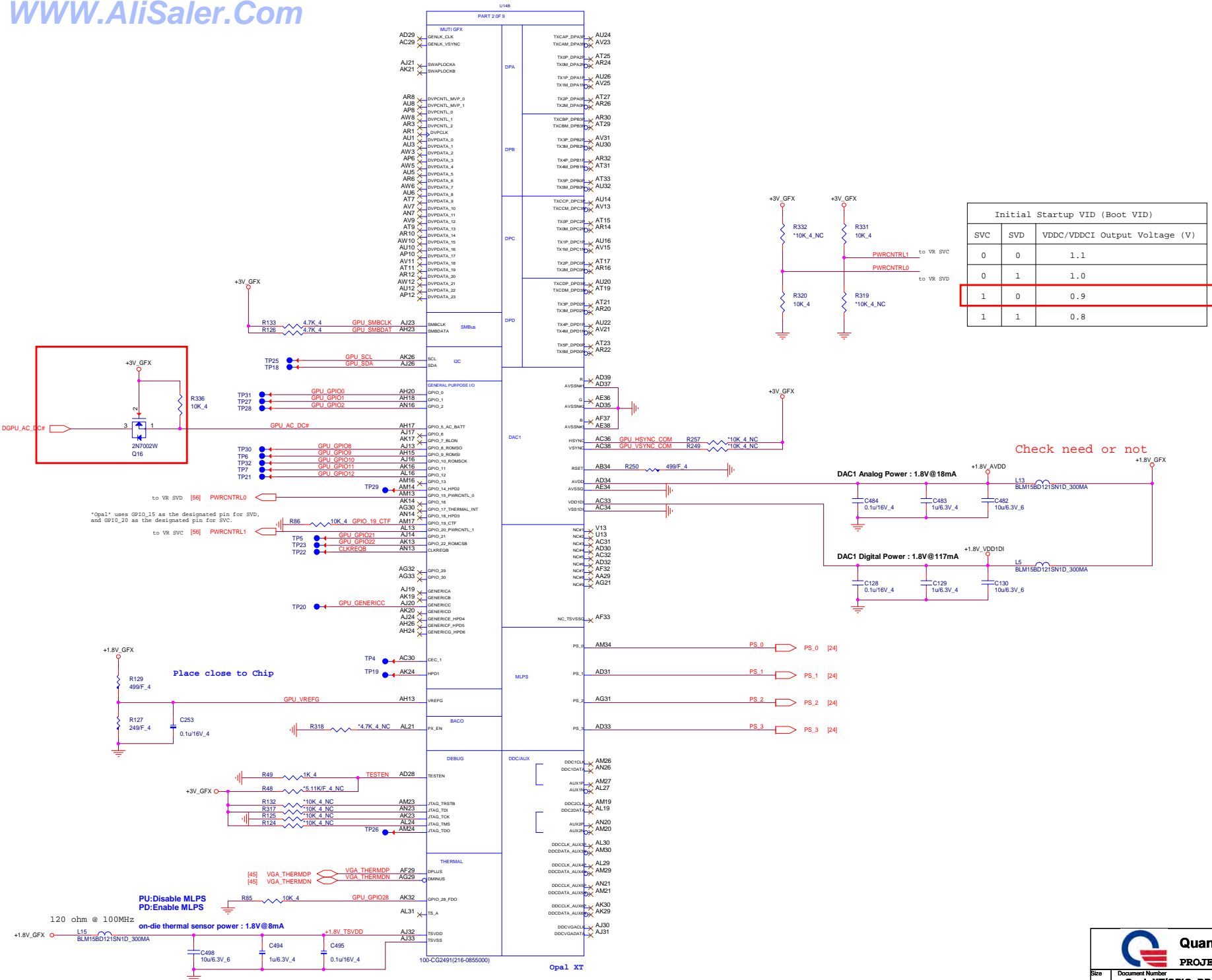
+3V_GFX/+1.8V_GFX/
+PCIE_VDDC_GFX(1.05V)/
+1.35V_GFX & +VGPU_CORE

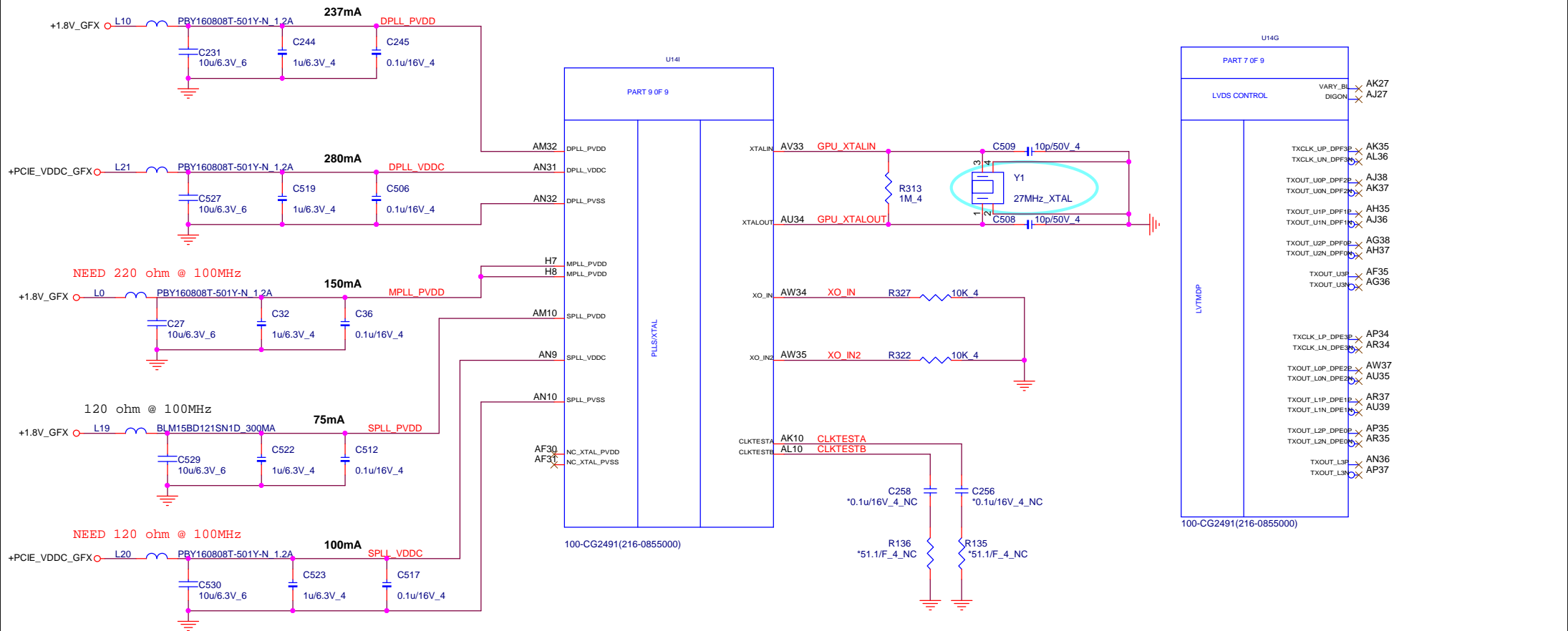
DGPU_PWROK


PERSTB
(DGPU_RST#)

PCIE Clock



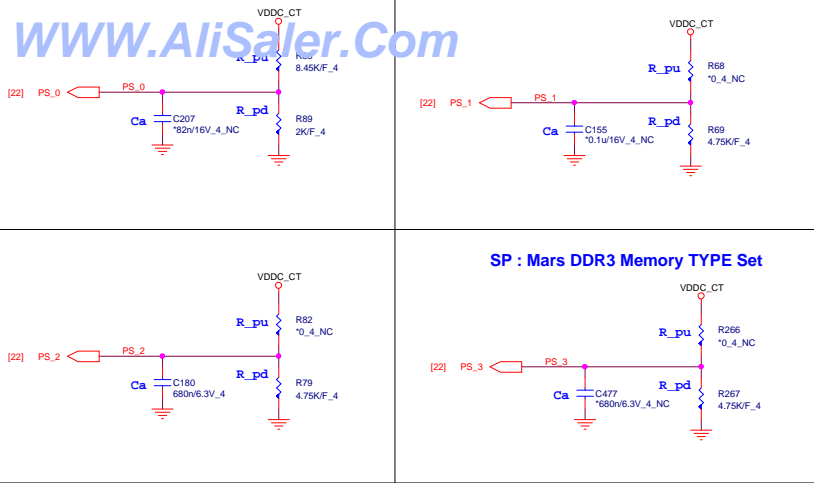






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MLPS Bit	Bits [5:1]
PS_0	11001
PS_1	11000
PS_2	00000
PS_3	11XXX

MLPS

Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	NA

R_pu	R_pd	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	10K	110
4.75K	NC	111

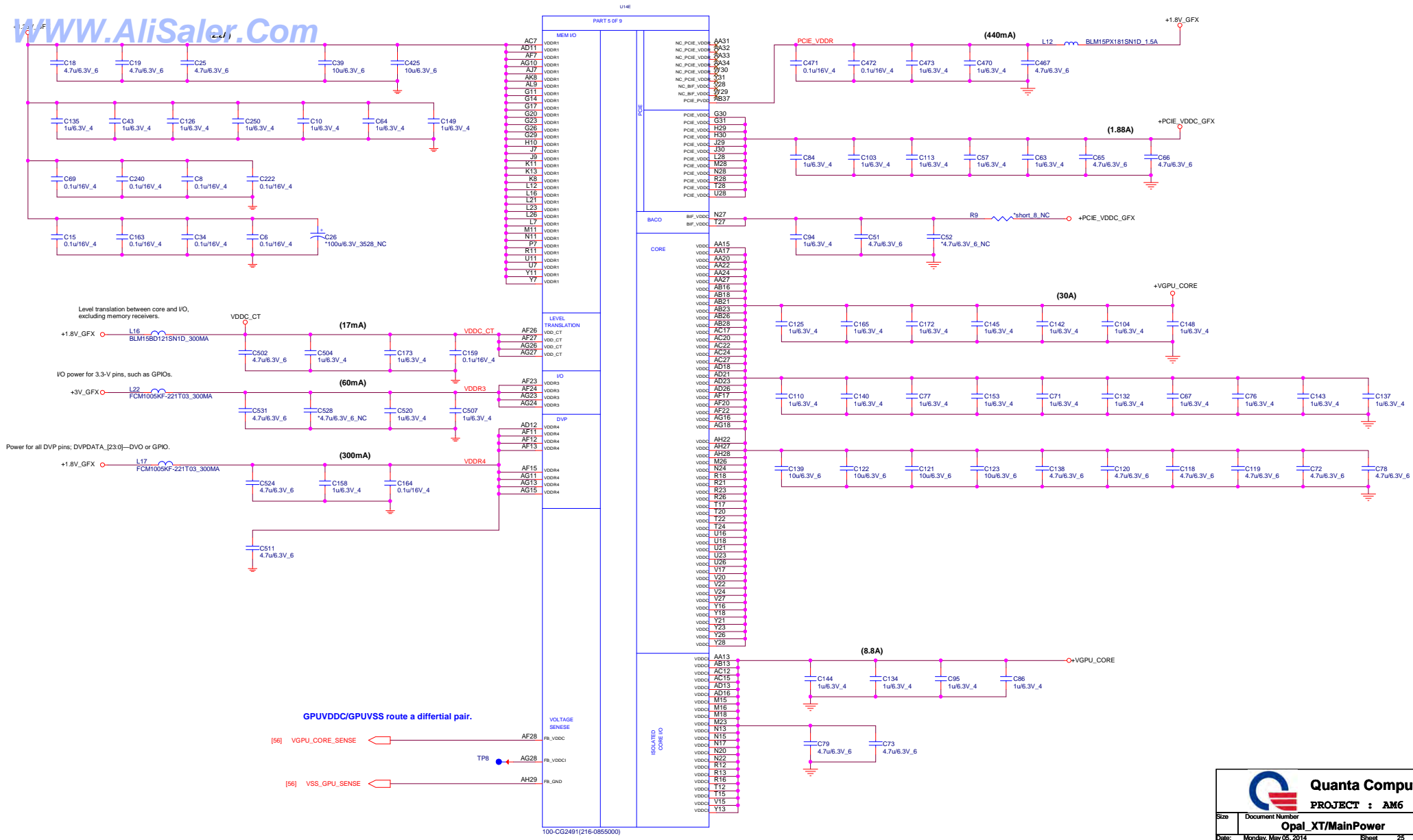
R_pu/R_pd	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
10K	CS31002FB26

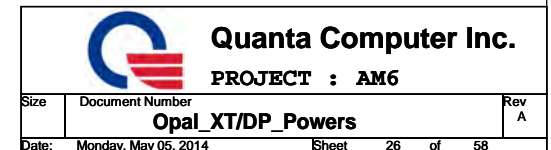
MLPS Bit	Strap Name	AM6 Settings	AM6 Settings	Description	AMD Recommended Settings
PS_0[1]	ROM_CONFIG[0]	1	Memory Aperture Size Select : 256MB	Serial ROM type or Memory Aperture Size Select If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size.	Design dependent, SIZE ROM_CONFIG[2:0] 128MB 000 256MB 001 64MB 010 Reserved 011
PS_0[2]	ROM_CONFIG[1]	0			
PS_0[3]	ROM_CONFIG[2]	0			
PS_0[4]	N/A	1	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	1	All endpoints are usable.	the strap option indicates the number of audio-capable display outputs.	Design dependent
PS_1[1]	STRAP_BIF_GEN3_EN_A	0	PCIe GEN3 is not supported. (use GEN2)	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent
PS_1[2]	STRAP_BIF_CLK_PM_EN	0	The CLKREQB power management capability is disabled	Determines whether or not the PCIe reference clock power management capability 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	0	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	1	The transmitter full-swing is enabled	Control the transmitter full-/half-swing mode 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	1	Tx deemphasis enabled.	PCI EXPRESS transmitter, deemphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent
PS_2[1]	N/A	0	Reserved.	Reserved.	N/A
PS_2[2]	N/A	0	Reserved.	Reserved.	N/A
PS_2[3]	STRAP_BIOS_ROM_EN	0	Disable the external BIOS ROM device.	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent
PS_2[4]	STRAP_BIF_VGA_DIS	0	Standalone dGPU design	VGA disable determines whether or not the card will be recognized as the system's VGA controller 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	Standalone dGPU design = 0 AMD PowerXpress design = 1
PS_2[5]	N/A	0	Reserved.	Reserved.	N/A
PS_3[1]	BOARD_CONFIG[0]	X	VRAM vendor BOARD_CONFIG[2:0] Hynix 000 default Micron 001 Samsung 010	Board configuration related strapping, such as for memory ID	Design dependent
PS_3[2]	BOARD_CONFIG[1]	X			
PS_3[3]	BOARD_CONFIG[2]	X			
PS_3[4]	AUD_PORT_CONN_PINSTRAP[1]	1	No usable endpoints.	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	Design dependent
PS_3[5]	AUD_PORT_CONN_PINSTRAP[2]	1			

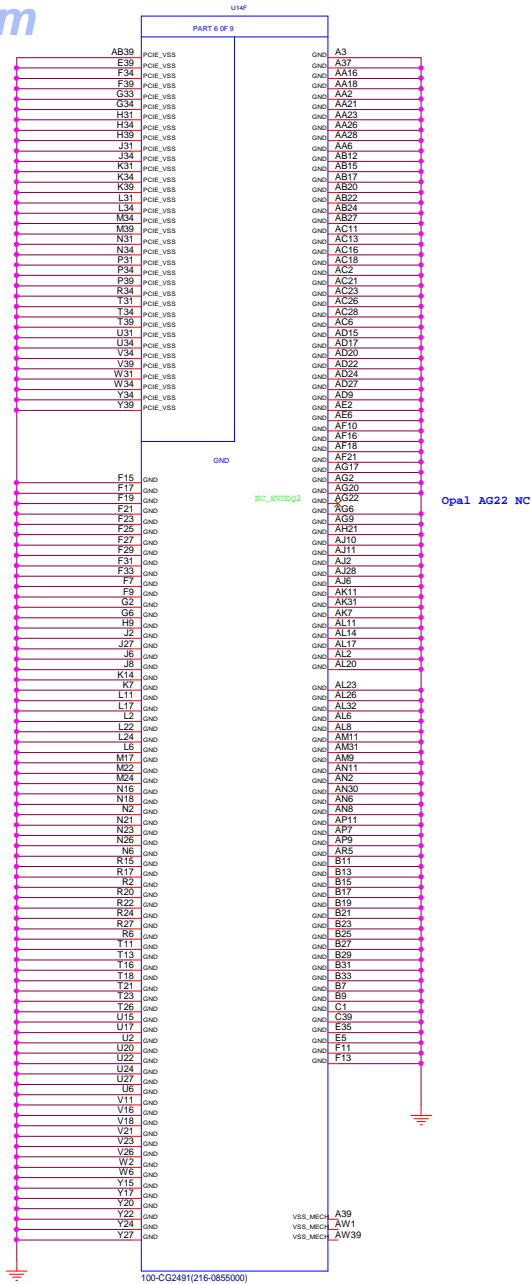
System Memory Aperture size

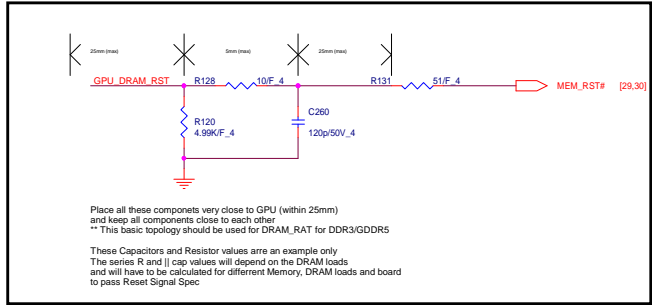
GPIO9 BIOSROM	SIZE	GPIO13 ROM_CONFIG2	GPIO12 ROM_CONFIG1	GPIO11 ROM_CONFIG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	Reserved	0	1	1

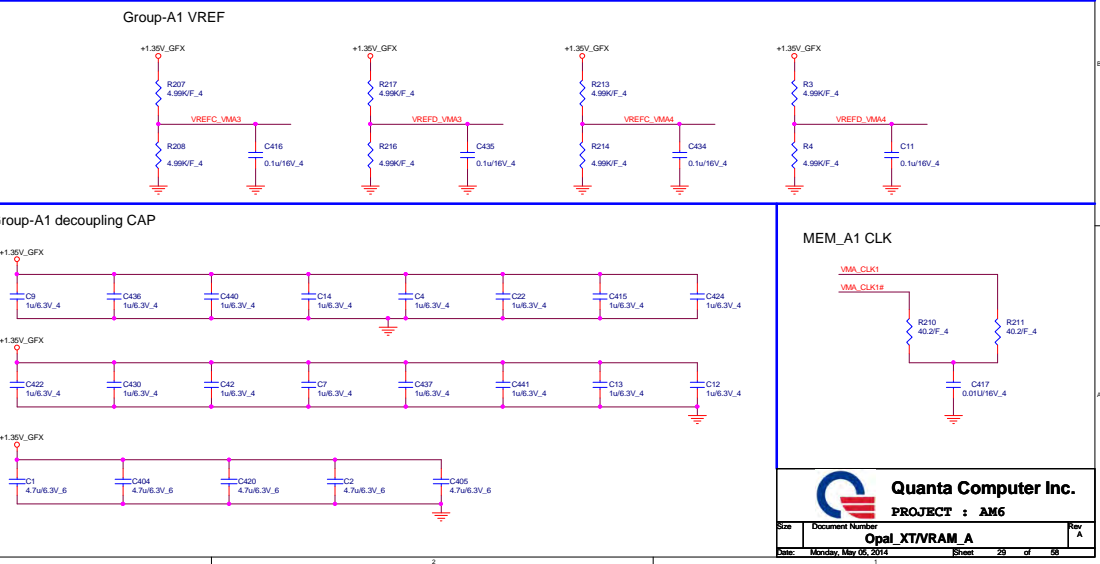
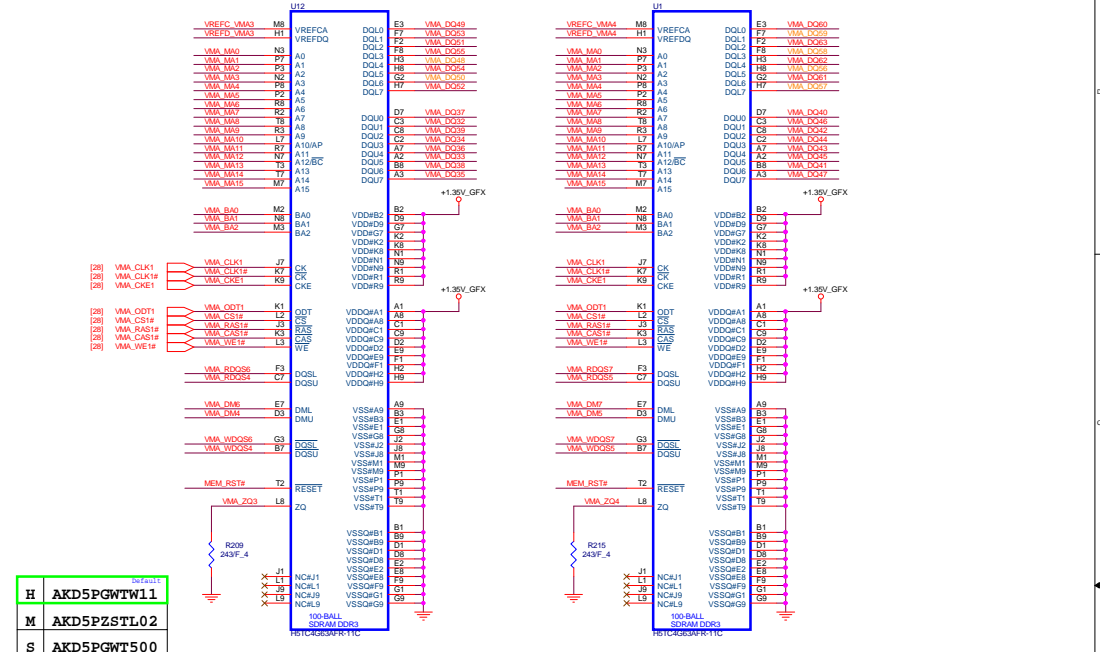
Vendor	Vendor P/N	STN B/S P/N	Size	MLPS
Hynix	H5TC4G63AFR-11C (256M*16)	AKD5PGWWTW11 * 8	4GB	000
Micron	MT41J256M16HA-093G:E (256M*16)	AKD5PZSTL02 * 8	4GB	001
Samsung	K4W4G1646D-BC1A (256M*16)	AKD5PGWT500 * 8	4GB	010

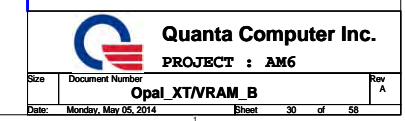


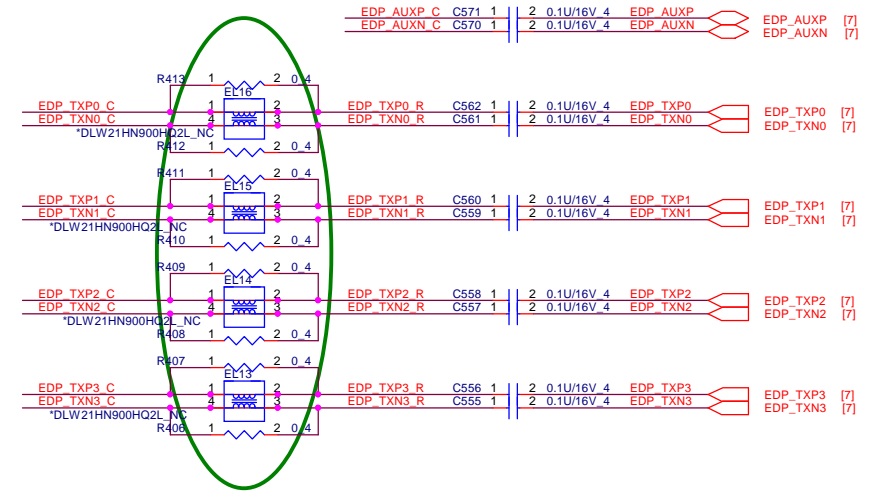
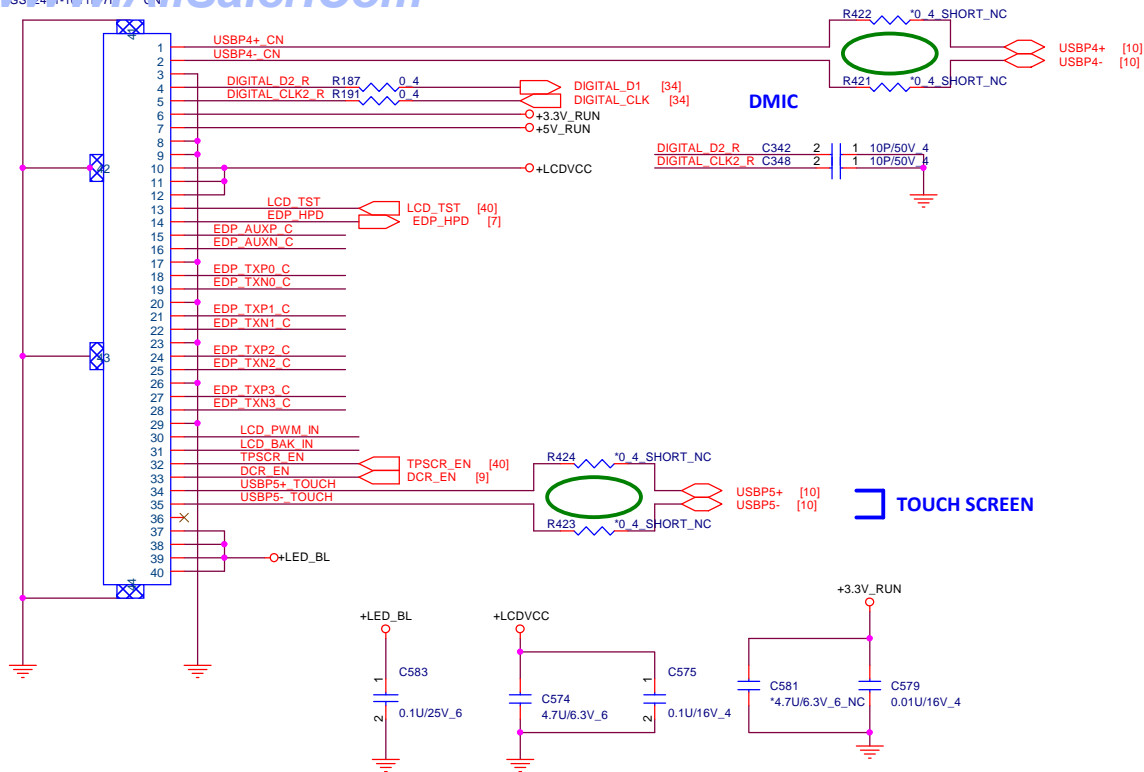




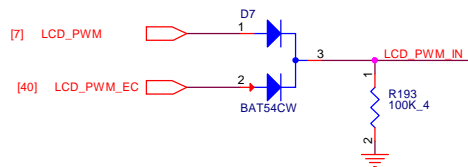




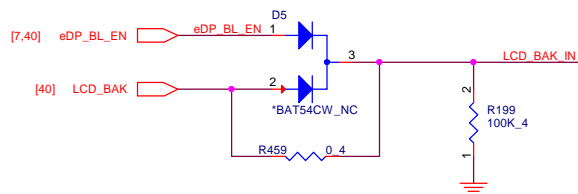




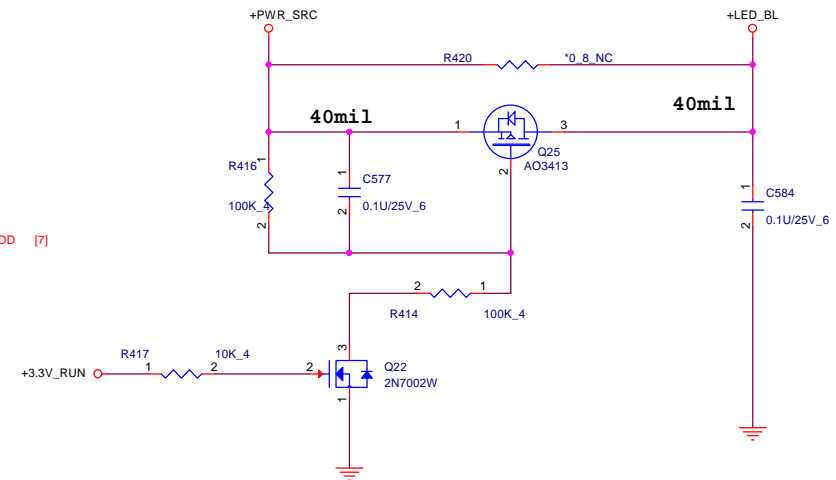
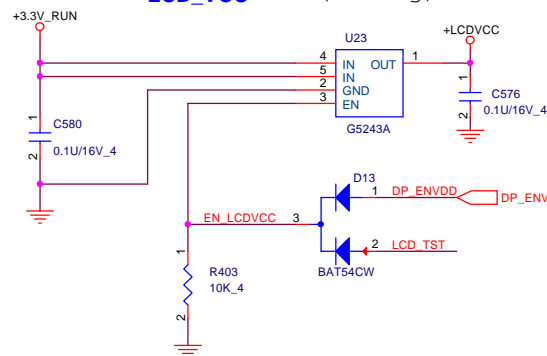
Brightness Control



BAK_EN

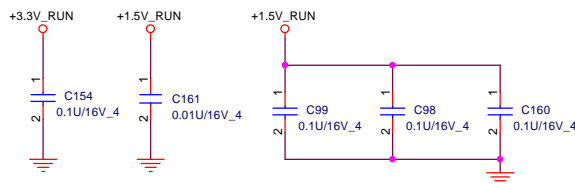
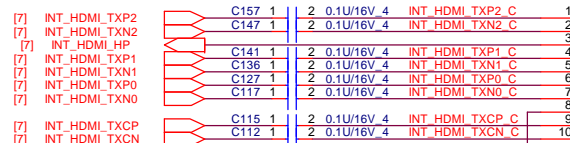
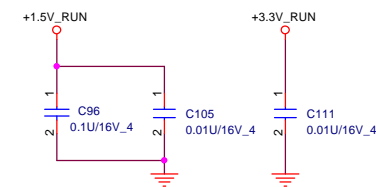


LCD_VCC Imax(ratting)=2.8A



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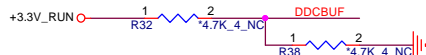
3 Level Input:
 L:LOW, internal pull down
 H:HIGH, external pull up
 M:(VDD3)/2, both external pull-up and pull-down

DC coupling enable



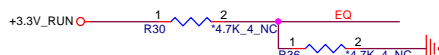
Int pull-down 150k , 3.3V IO
 L:default, AC coupling input
 H:DC coupling input

enable active DDC buffer

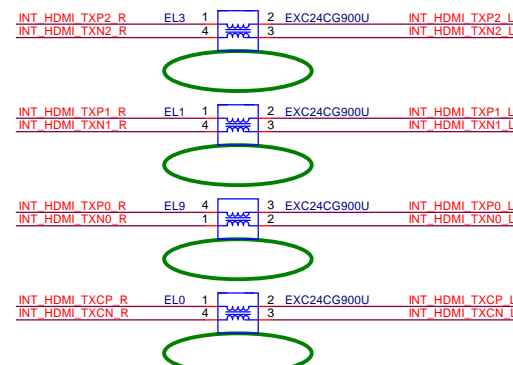
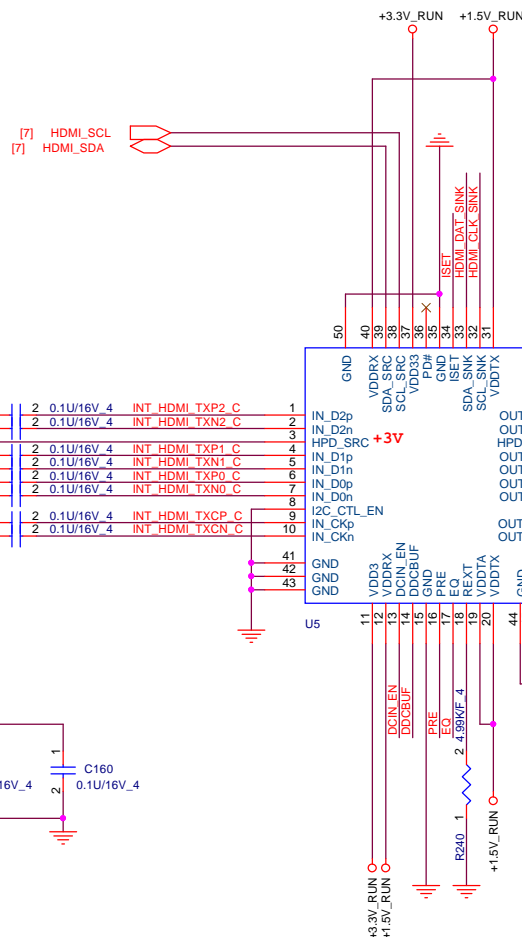


Int pull-down 150k , 3.3V IO
 L:default, passive DDC pass-through without internal pull up
 H:active DDC buffer with internal pull up
 M:active DDC buffer without internal pull up

Receiver equalization setting



Int pull-down 150k , 3.3V IO
 L:programmable EQ for channel loss up to 12.4dB
 H:programmable EQ for channel loss up to 4.3dB
 M:programmable EQ for channel loss up to 8.6dB

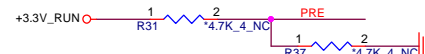


configuration pin



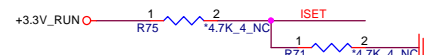
Int pull-down 150k , 3.3V IO
 L:HDMI ID disable
 H:HDMI ID enable

Output pre-emphasis setting



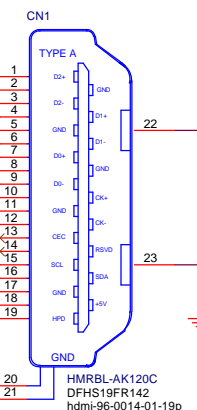
Int pull-down 150k , 3.3V IO
 L:no pre-emphasis
 H:1.6dB pre-emphasis
 M:2.5dB pre-emphasis

TMDS output swing adjustment



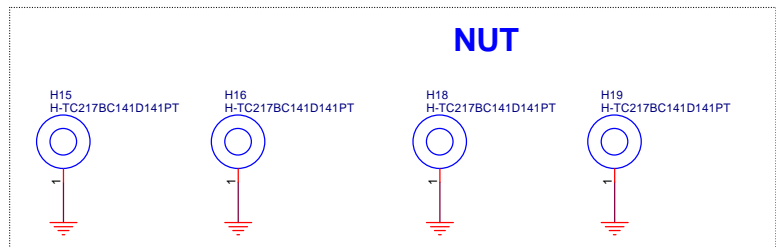
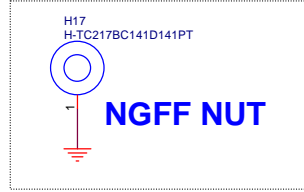
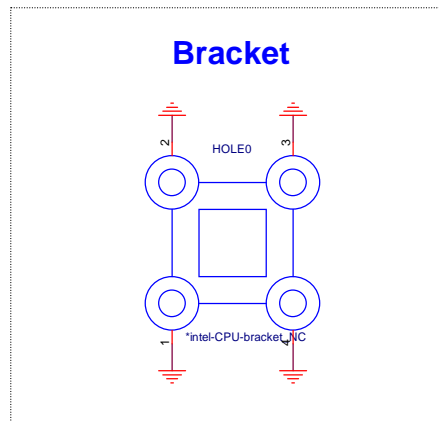
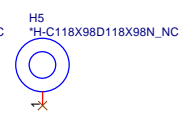
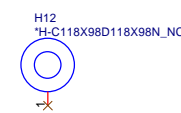
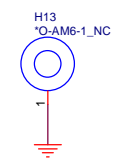
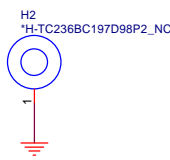
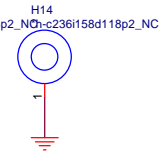
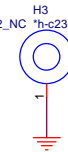
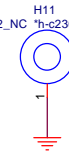
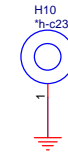
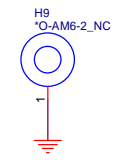
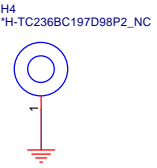
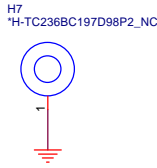
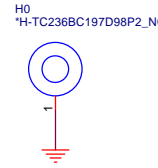
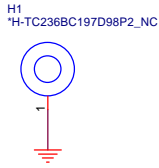
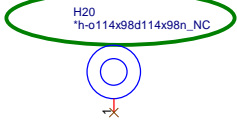
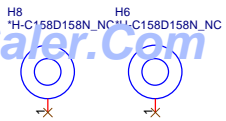
Int pull-down 150k , 3.3V IO
 L:default
 H:increase +13%
 M:increase -13%

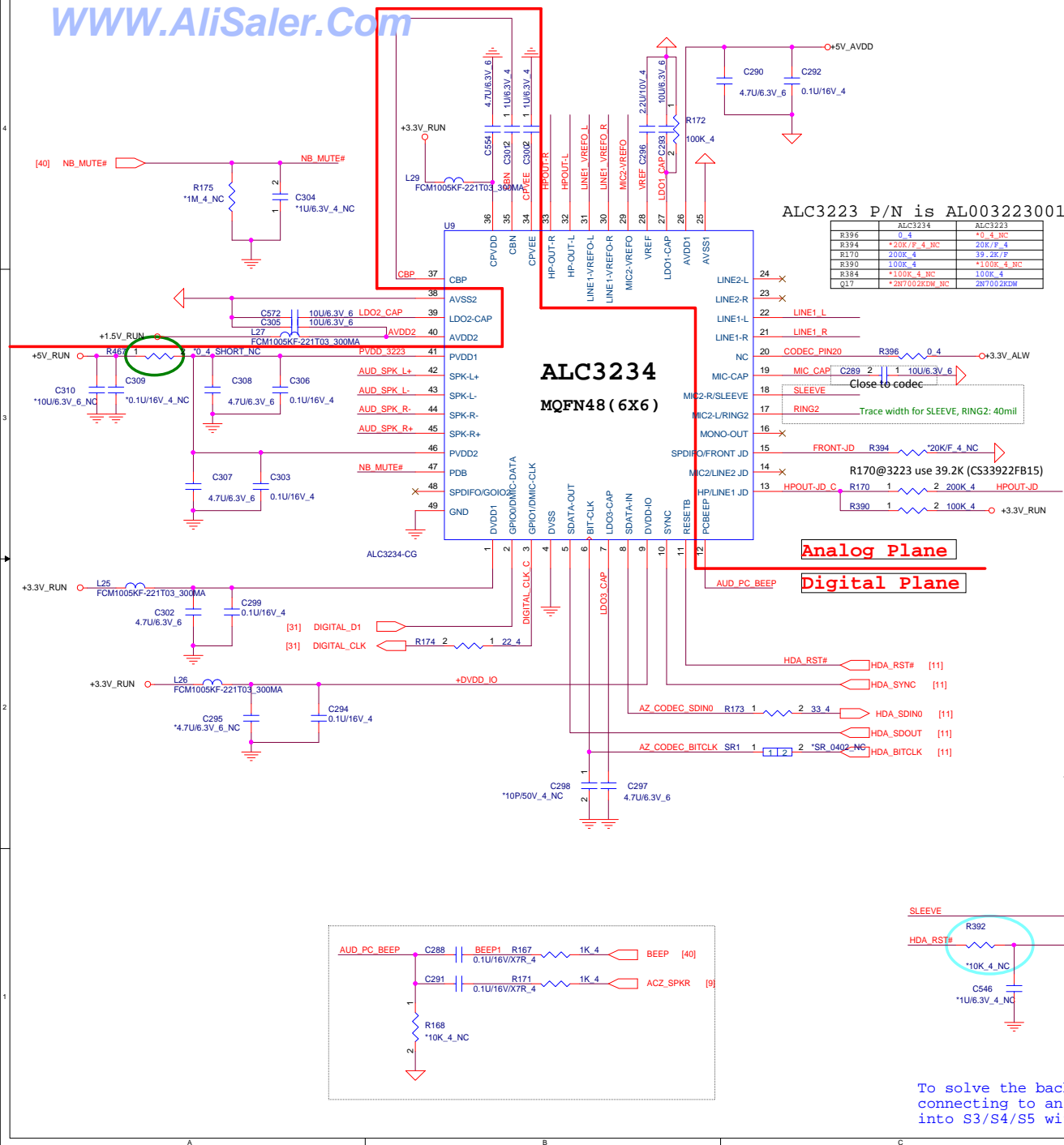
HDMI CN



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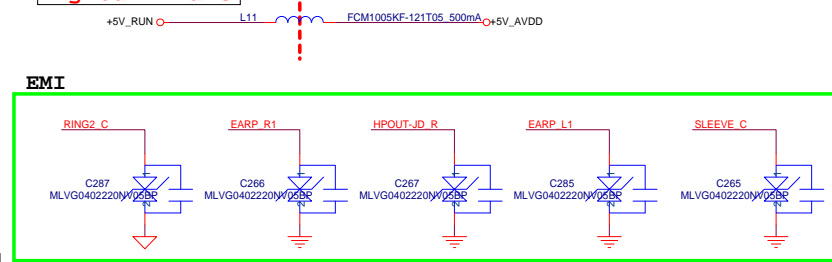
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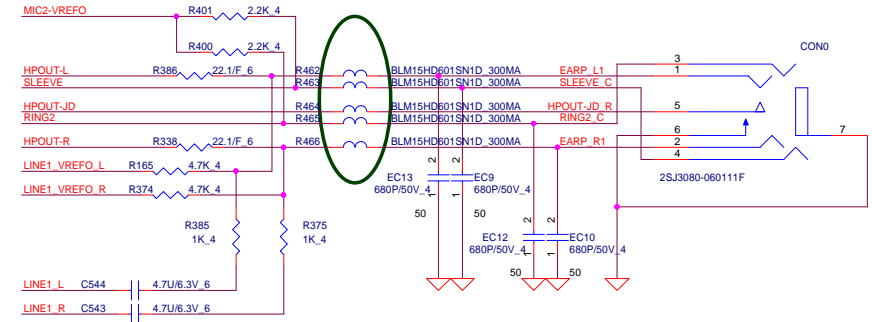


Digital Plane

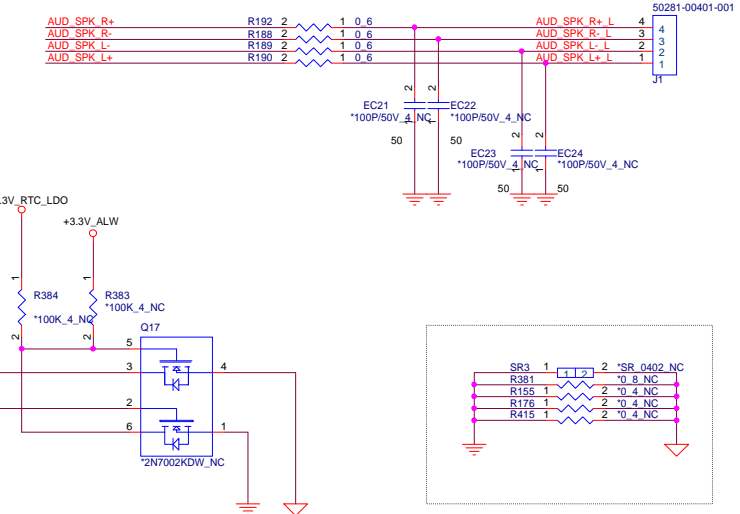
Analog Plane



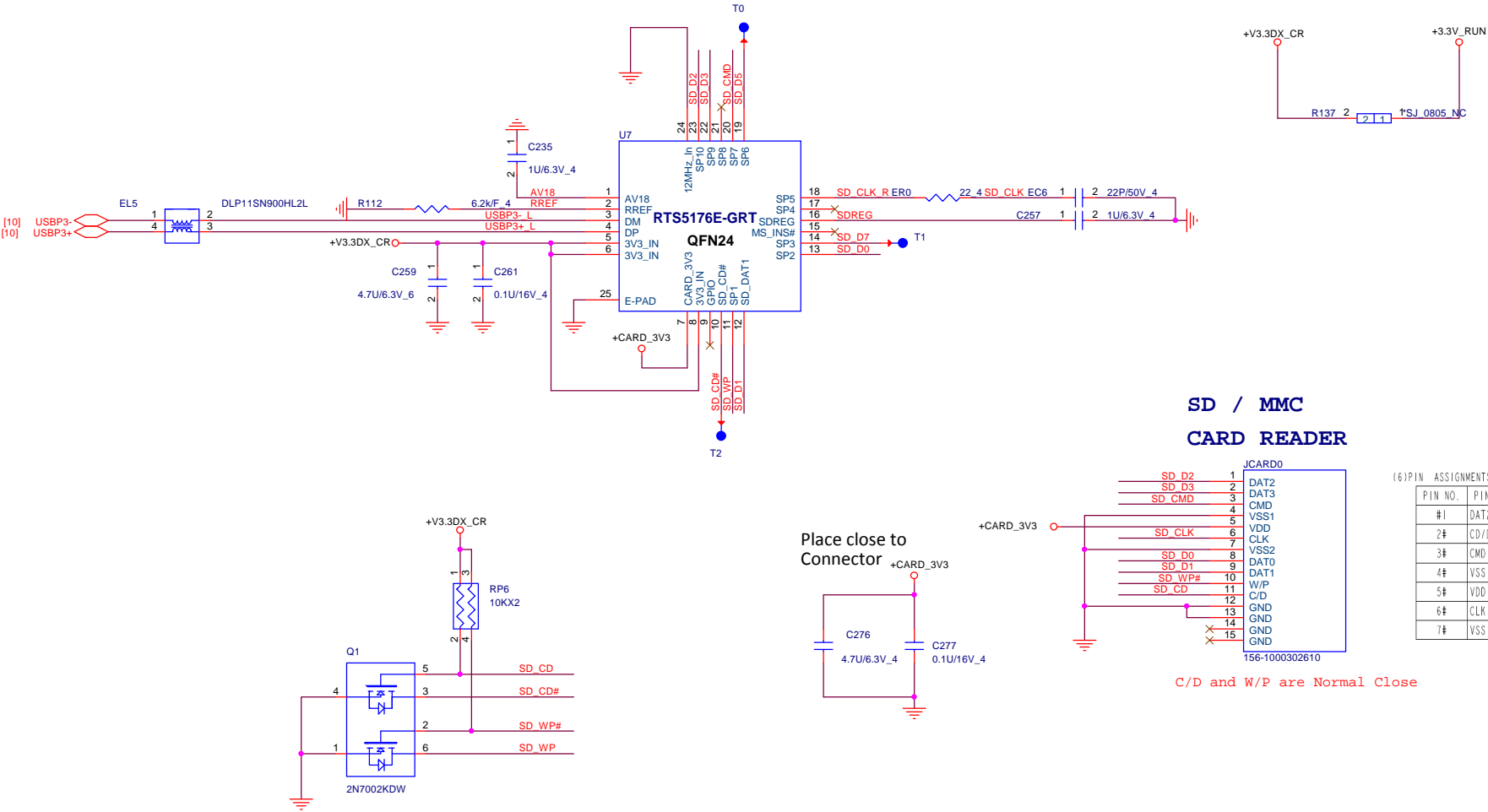
Universal Audio Jack
(ALC3223 supported iPhone/Nokia headset
, Headphone, Line-In and Microphone)



0802 Chang R171,R225 P/N to CS24702JB38(4.7k)



To solve the background noise while combojack connecting to an active speaker and system entry into S3/S4/S5 without analog power



SD / MMC
CARD READER

(6) PIN ASSIGNMENTS

PIN NO.	PIN DEFINE	PIN NO.	PIN DEFINE
1#	DAT2	8#	DAT0
2#	CD/DAT3	9#	DAT1
3#	CMD	10#	WP SW
4#	VSS	11#	CD SW
5#	VDD	12#	GND SW
6#	CLK	13#	GND SW
7#	VSS		

C/D and W/P are Normal Close

USB3.0 Power Share

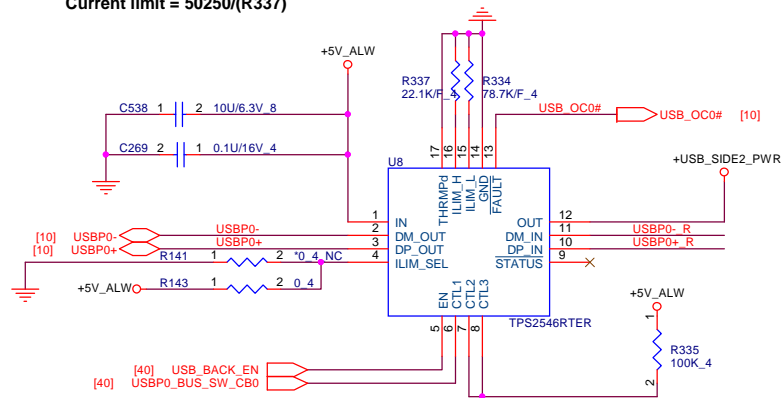
USB Power share

USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.2

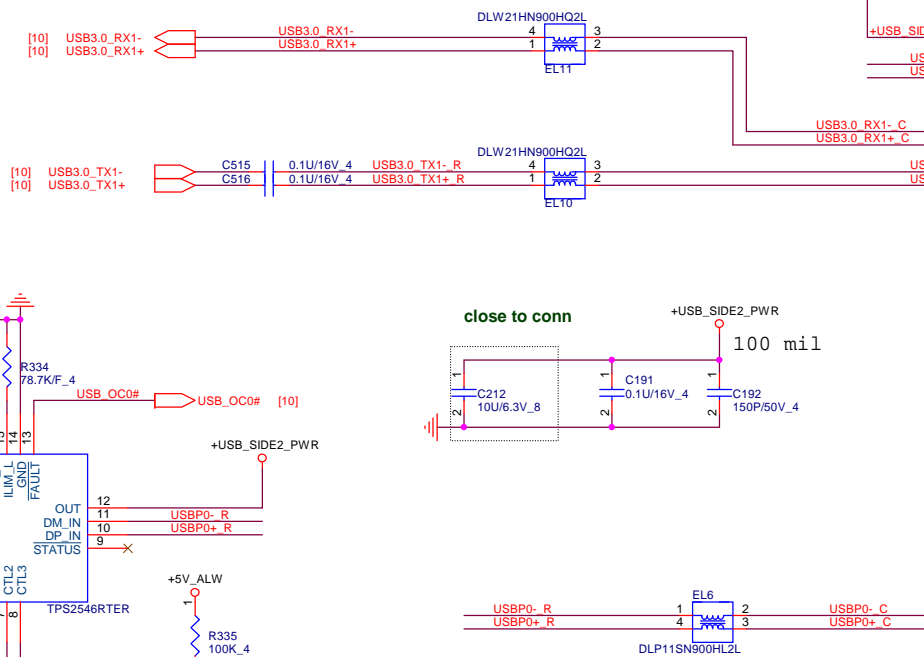
	R337	mA
OC limitation	100k ohm	504
	22.1k ohm	2274

Applied Now

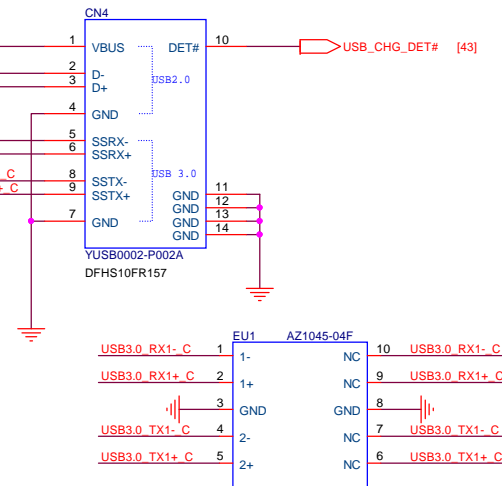
Current limit = 50250/(R337)



USB3.0/2.0 COMBO X 1

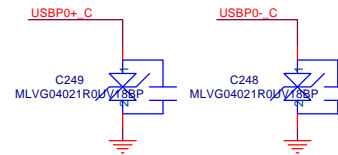


USB 3.0



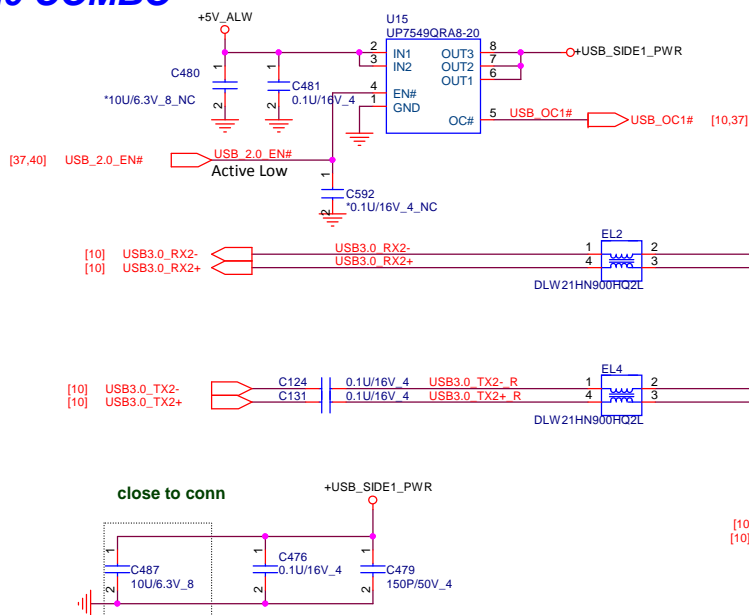
ESD Function

Place ESD diodes as close as USB connector.

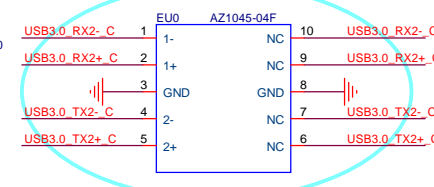


USB3.0/2.0 COMBO

M15 Design Requirement:
I continuous 1.5A ; OC 2.0A

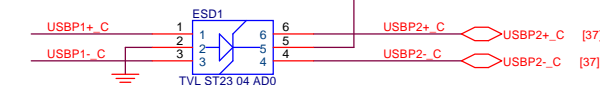


USB 3.0



ESD Function

Place ESD diodes as close as USB connector.

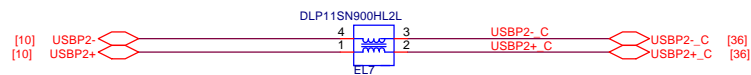
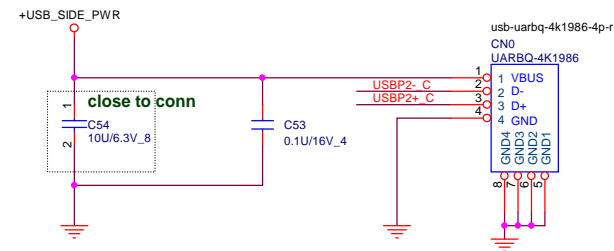
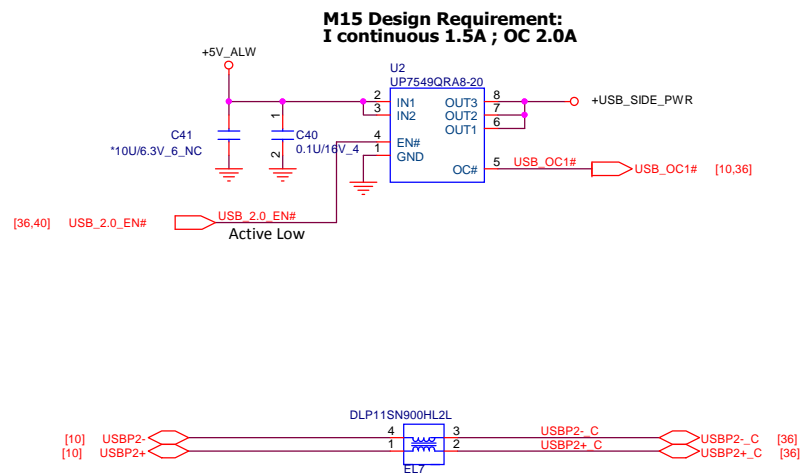


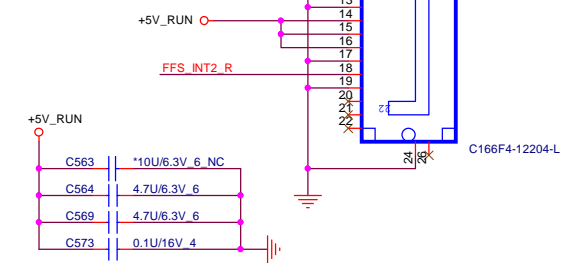
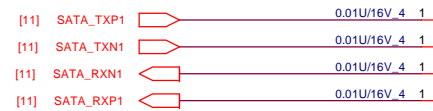
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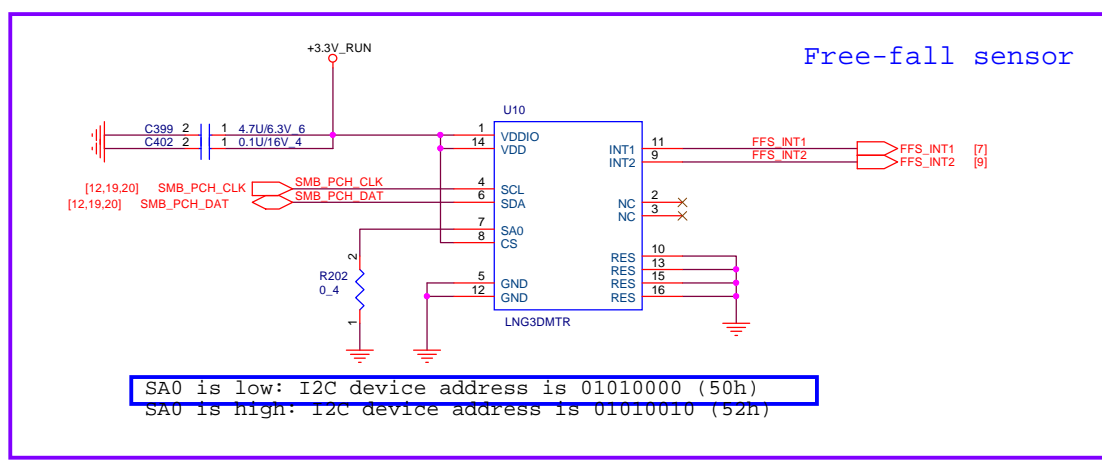
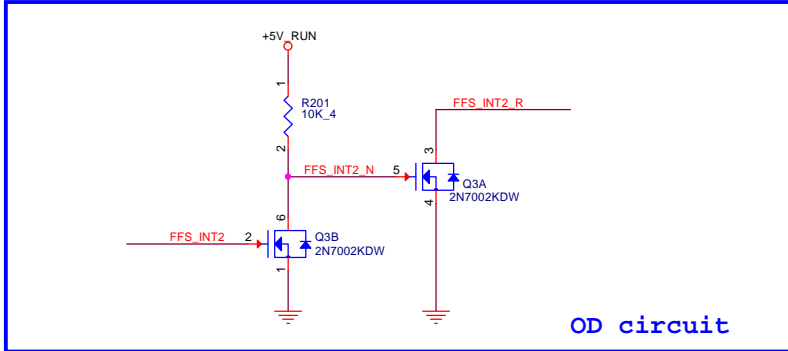
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USB2.0 X1

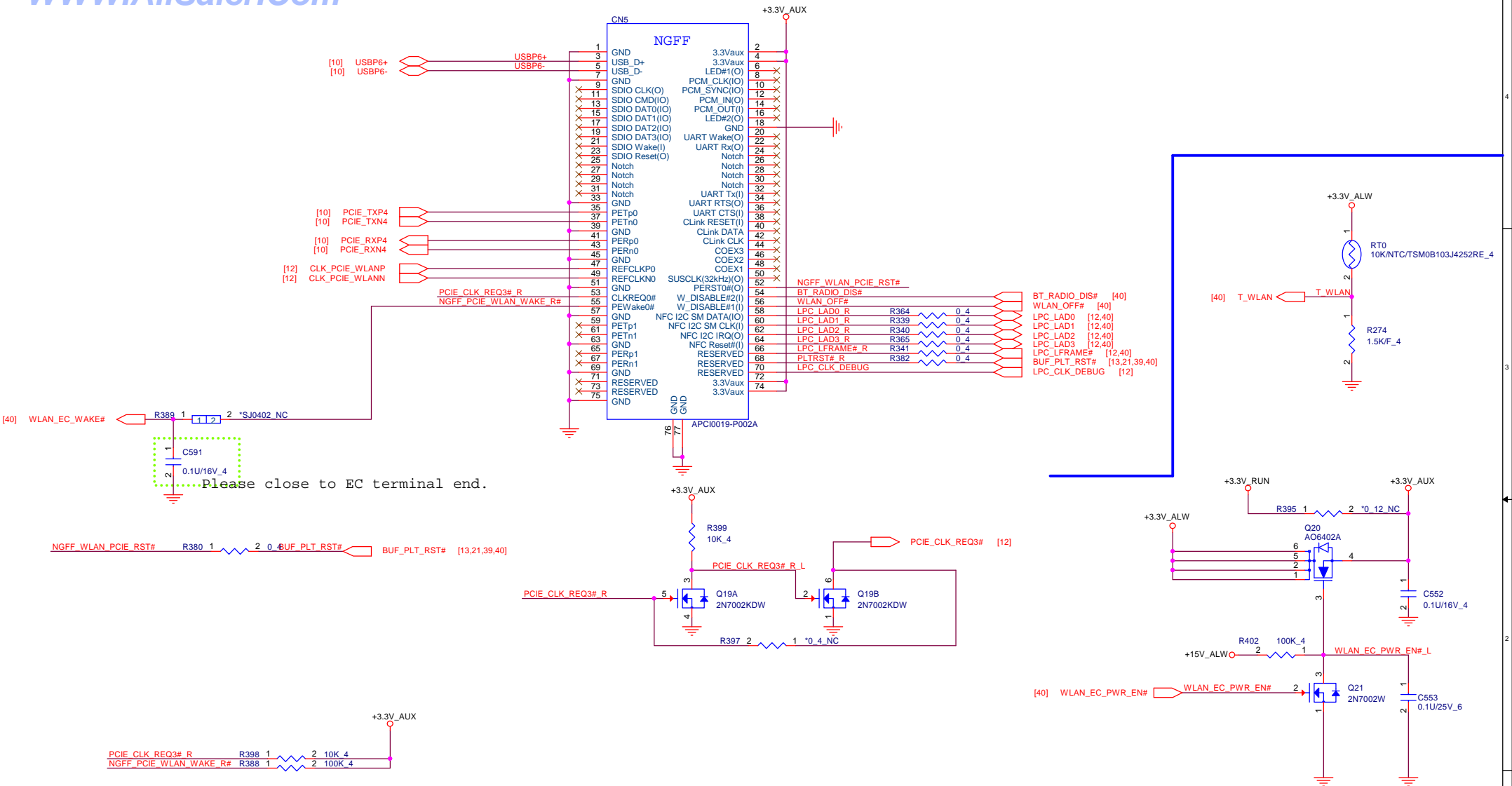




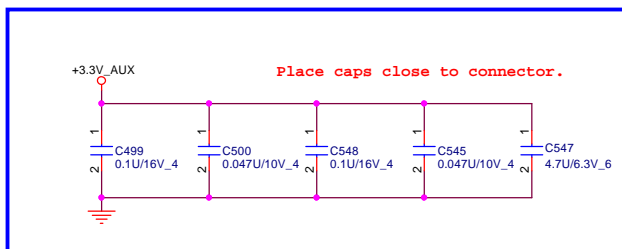
If you have two HDD,need add two OD circuit for Fall sensor interrupt circuit

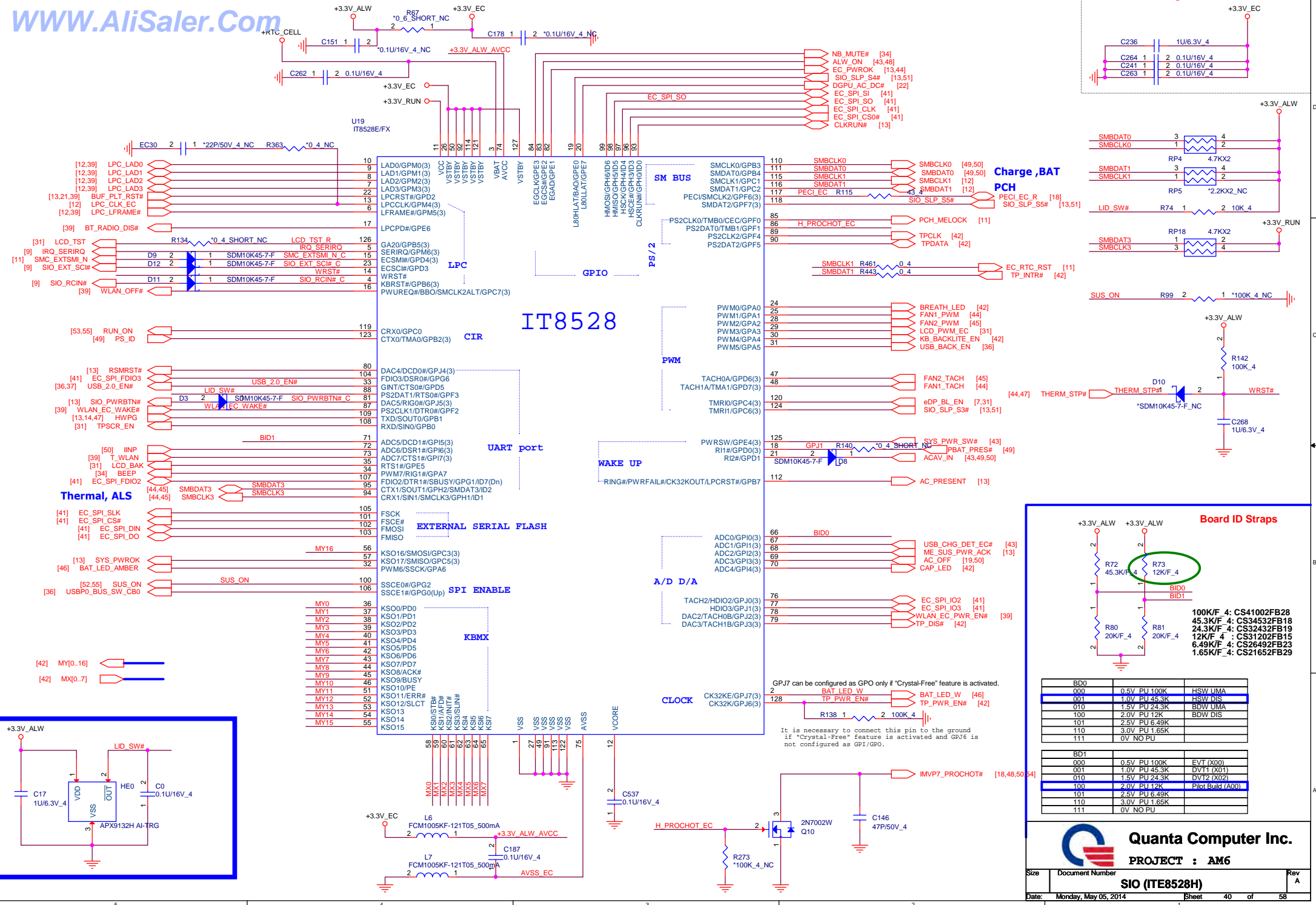


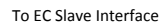
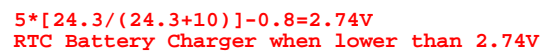
NGFF Wifi/BT connector



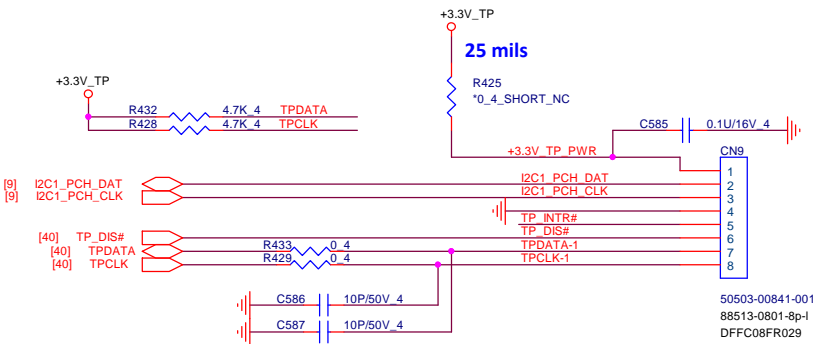
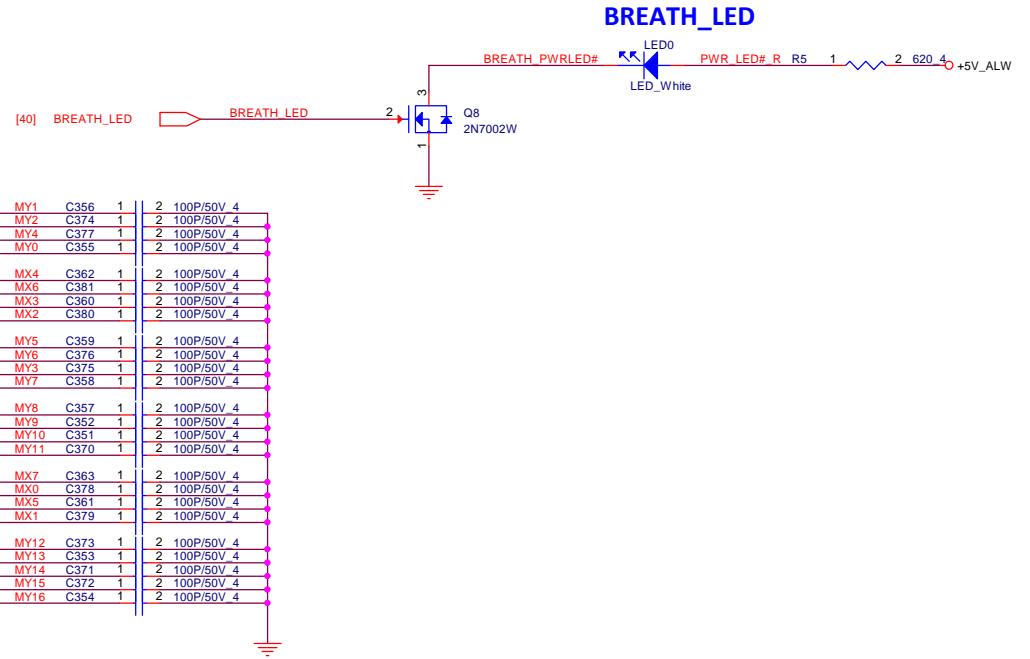
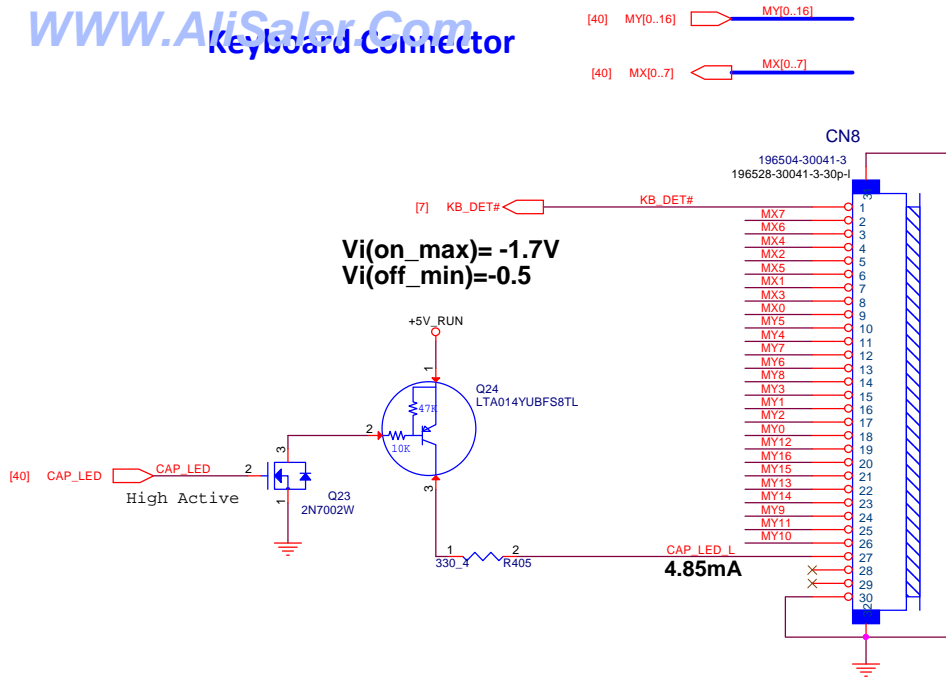
Support AOAC on WLAN





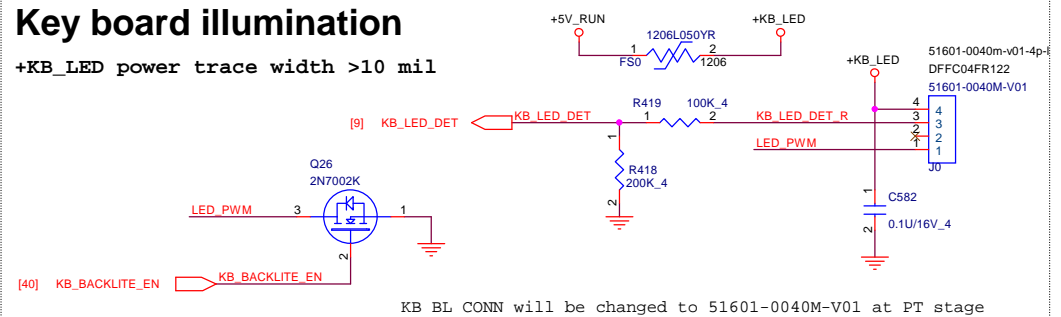


Keyboard Connector

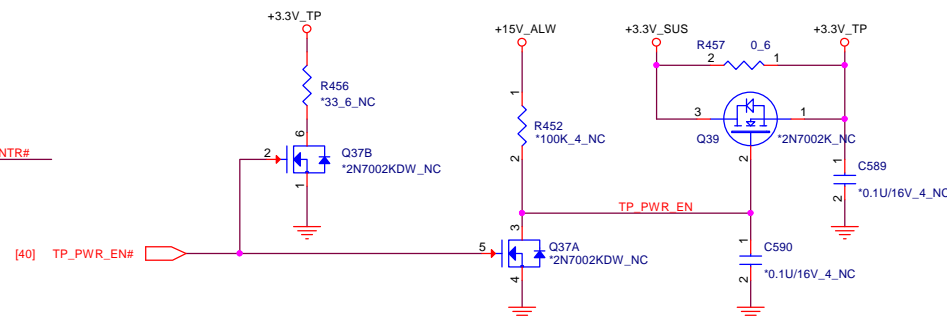
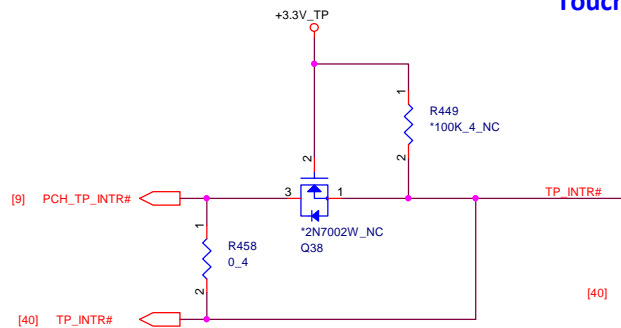


Key board illumination

+KB_LED power trace width >10 mil



Touch Pad Connector



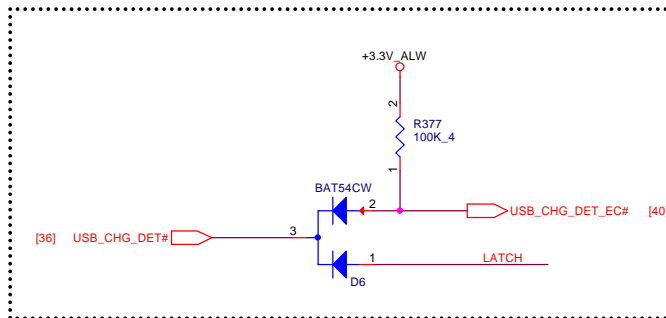
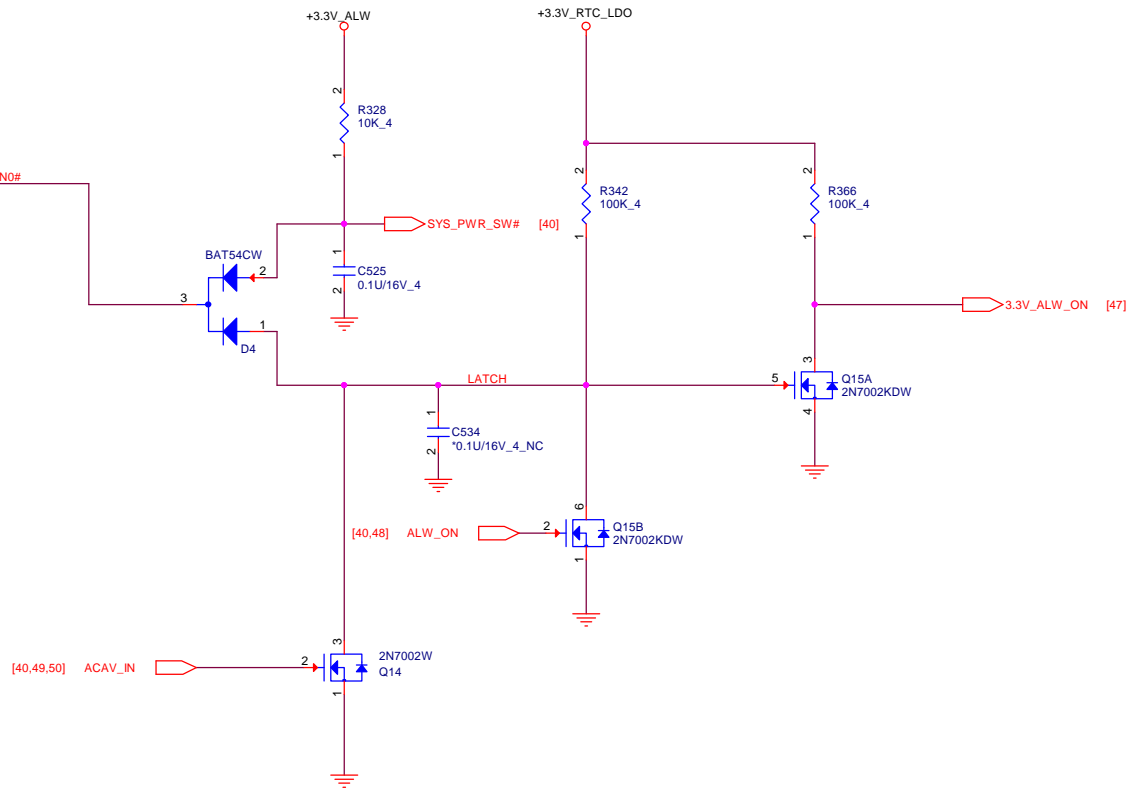
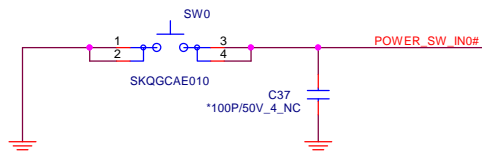
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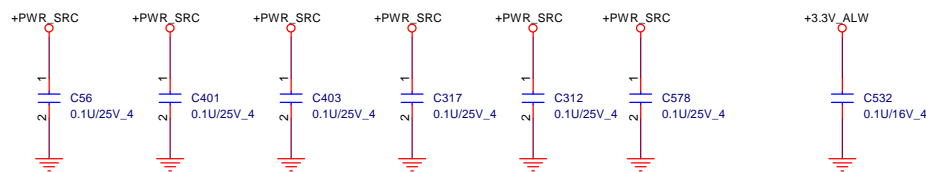
KB/CLK Gen/FAN/TP

3VALW ON POWER LOGIC

POWER BUTTON



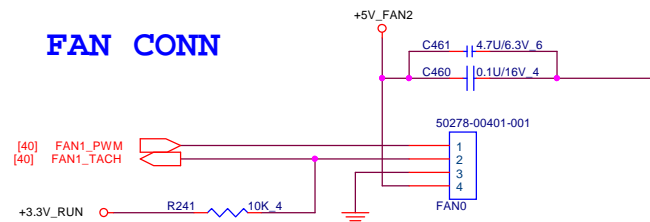
Stitching Capacitors



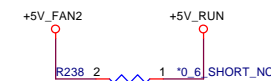
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FAN CONN

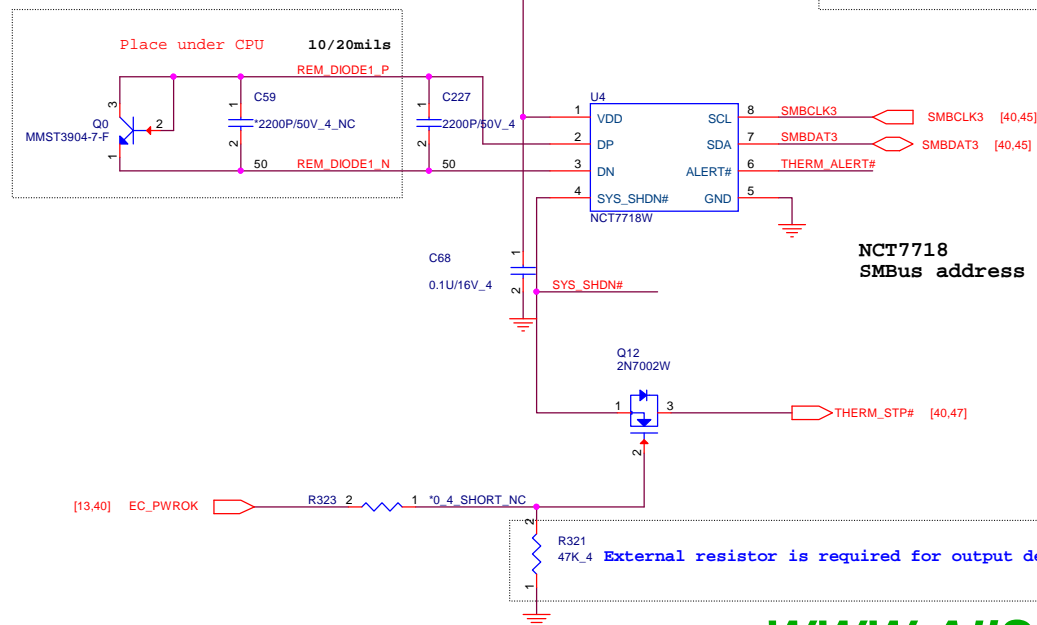


+5V_FAN
Max Current : mA

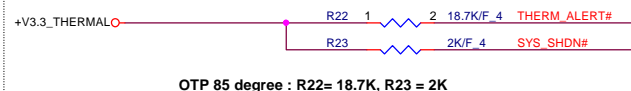


THERMAL IC

Need closed to CPU



OTP 85 degree C

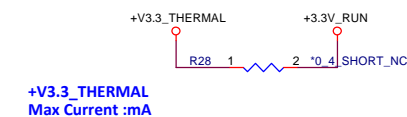


OTP 85 degree : R22= 18.7K, R23 = 2K

NCT7718

SMBus address is 1001100xb (98h) (x is R/W bit).

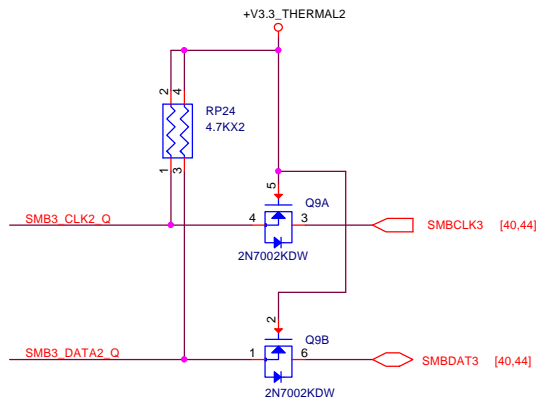
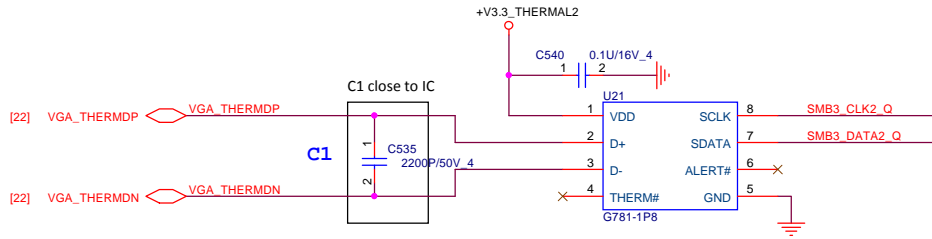
SYS_SHDN#	2K	7.5K	10.5K	14K	18.7K
ALERT#					
2K	77'C	87'C	97'C	107'C	117'C
7.5K	79'C	89'C	99'C	109'C	119'C
10.5K	81'C	91'C	101'C	111'C	121'C
14K	83'C	93'C	103'C	113'C	123'C
18.7K	85'C	95'C	105'C	115'C	125'C



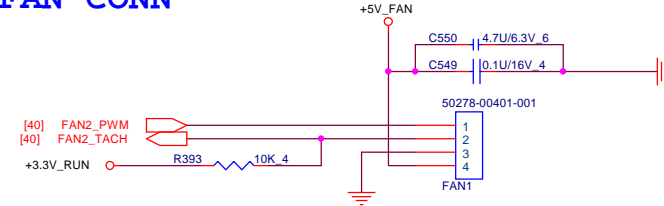
Quanta Computer Inc.

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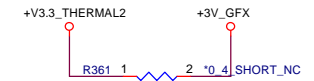
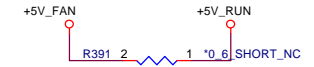
G781-1P8
SMBus address is 1001101xb (9Ah) (x is R/W bit).



FAN CONN



+5V_FAN
Max Current : mA

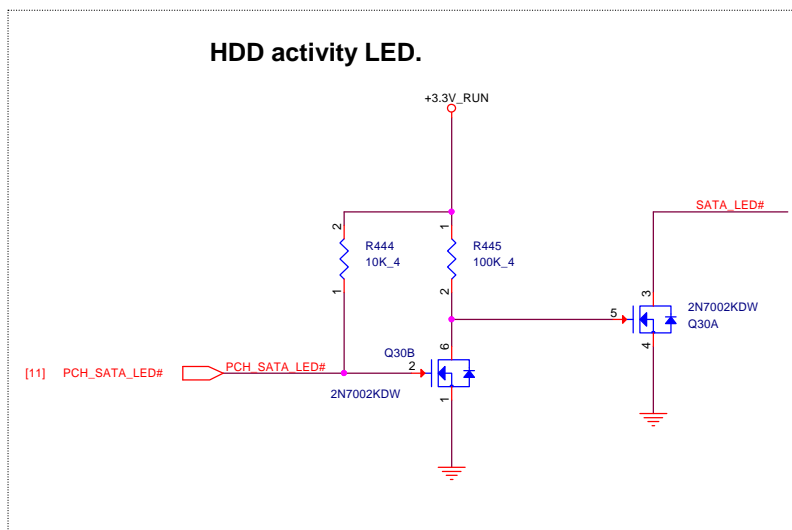
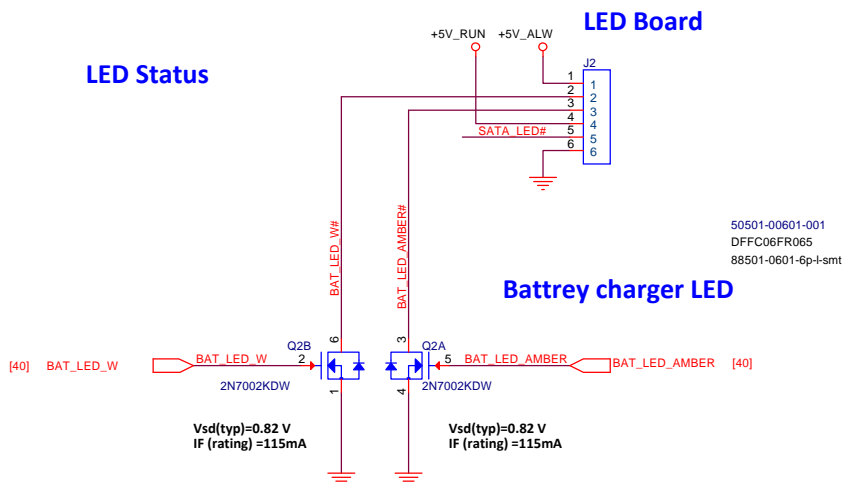


+V3.3_THERMAL
Max Current :mA



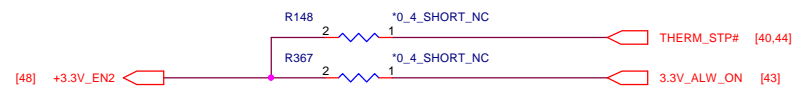
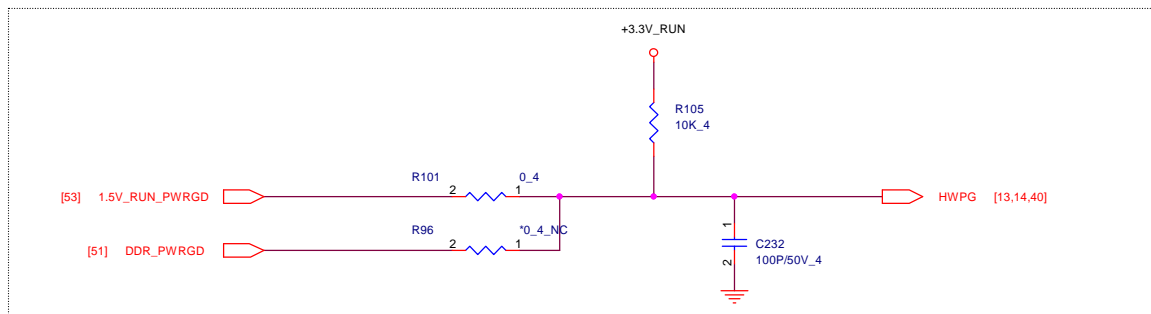
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	Thermal GPU	A
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	LED	A
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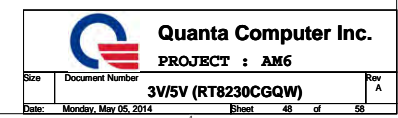


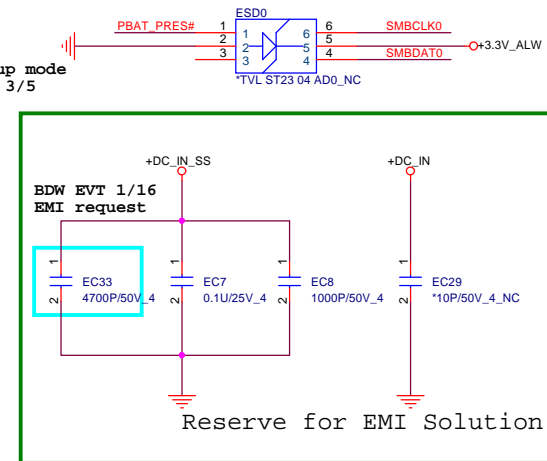
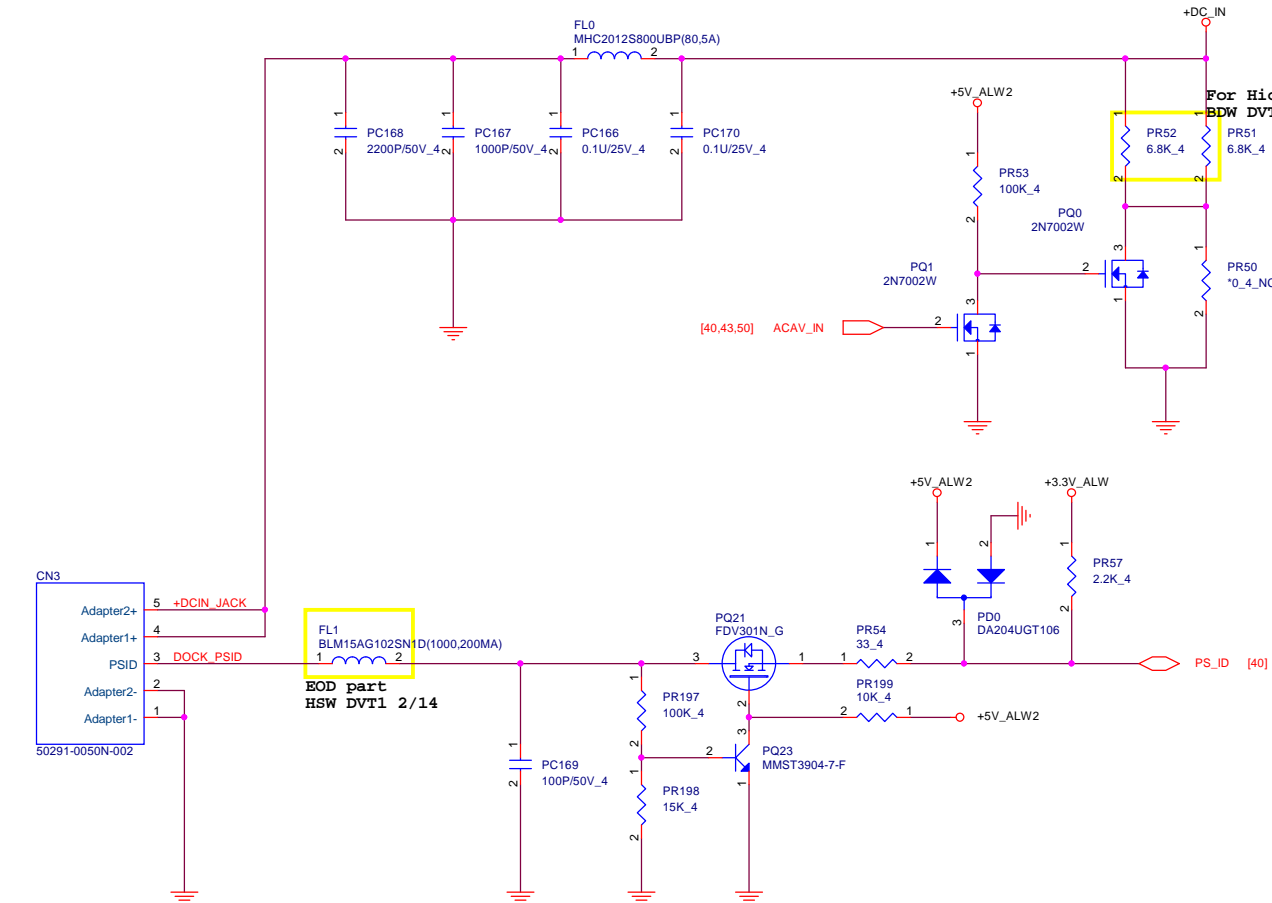
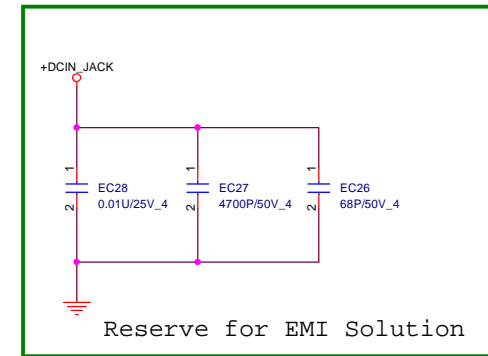
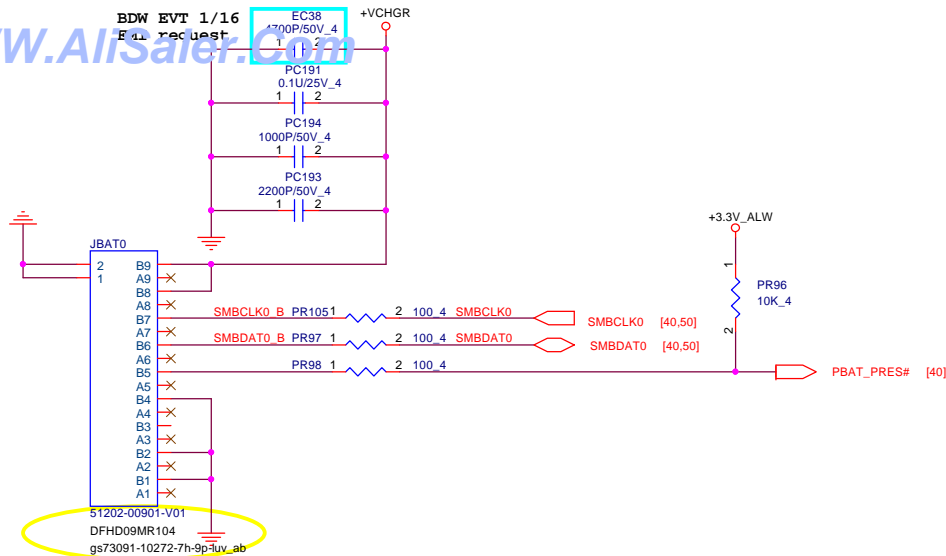
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System Reset Circuit

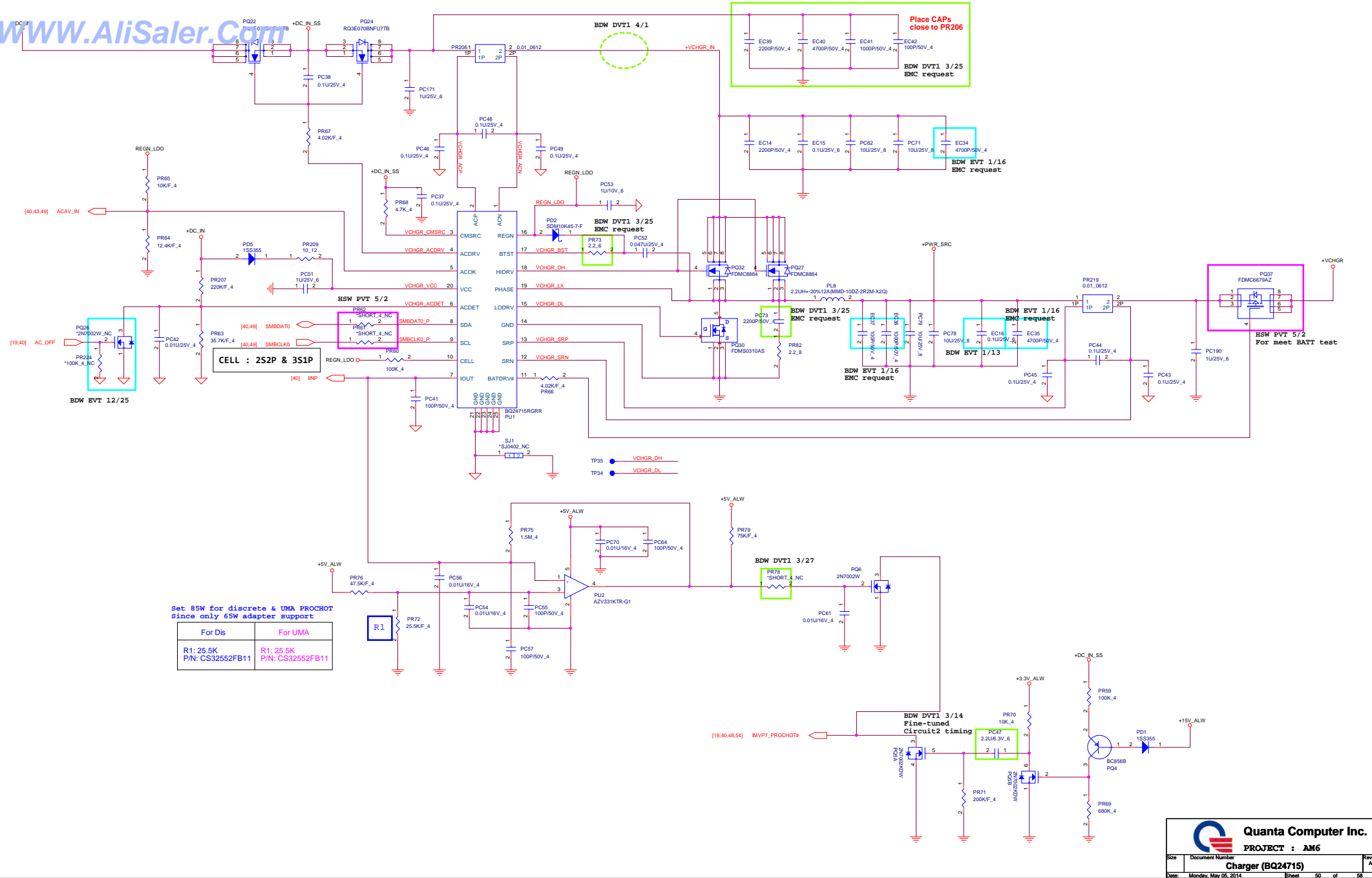
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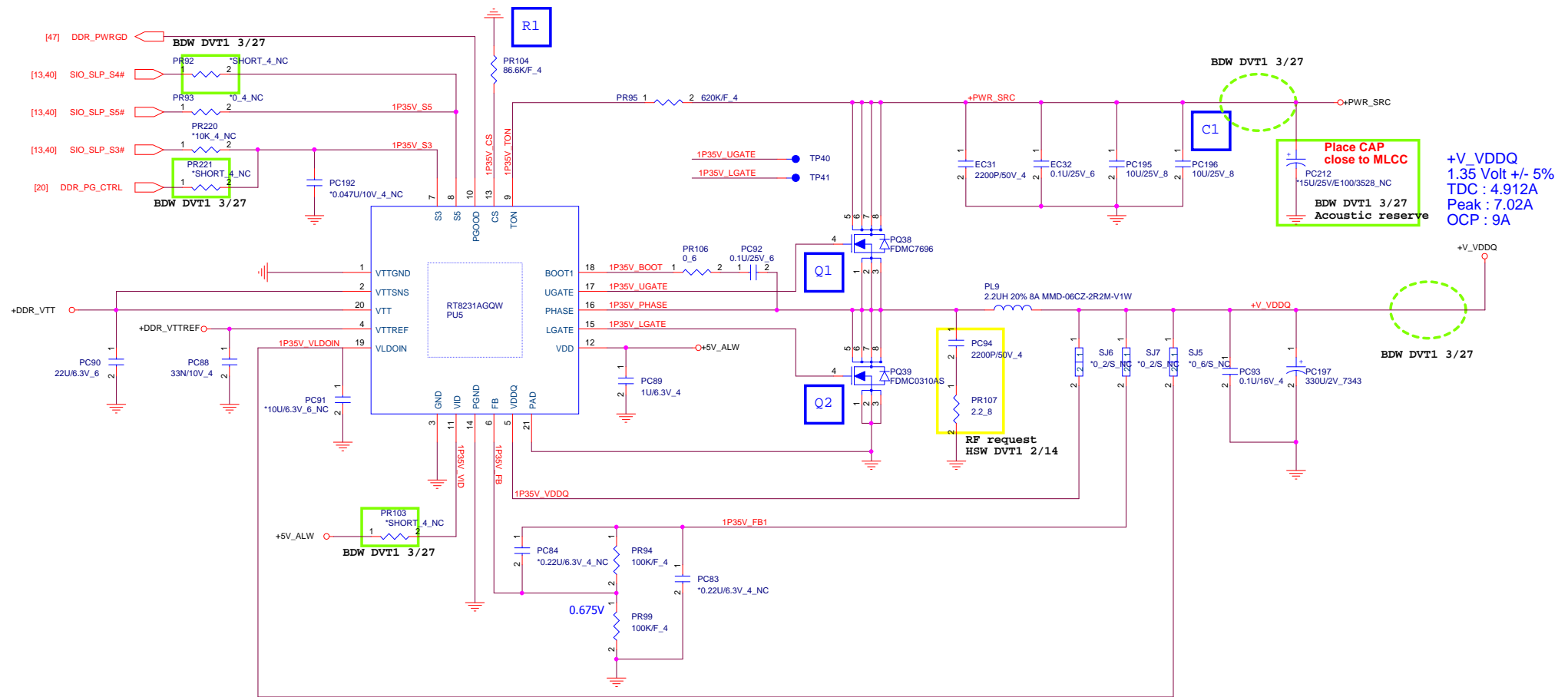


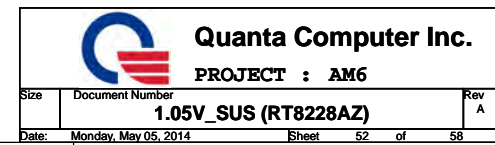


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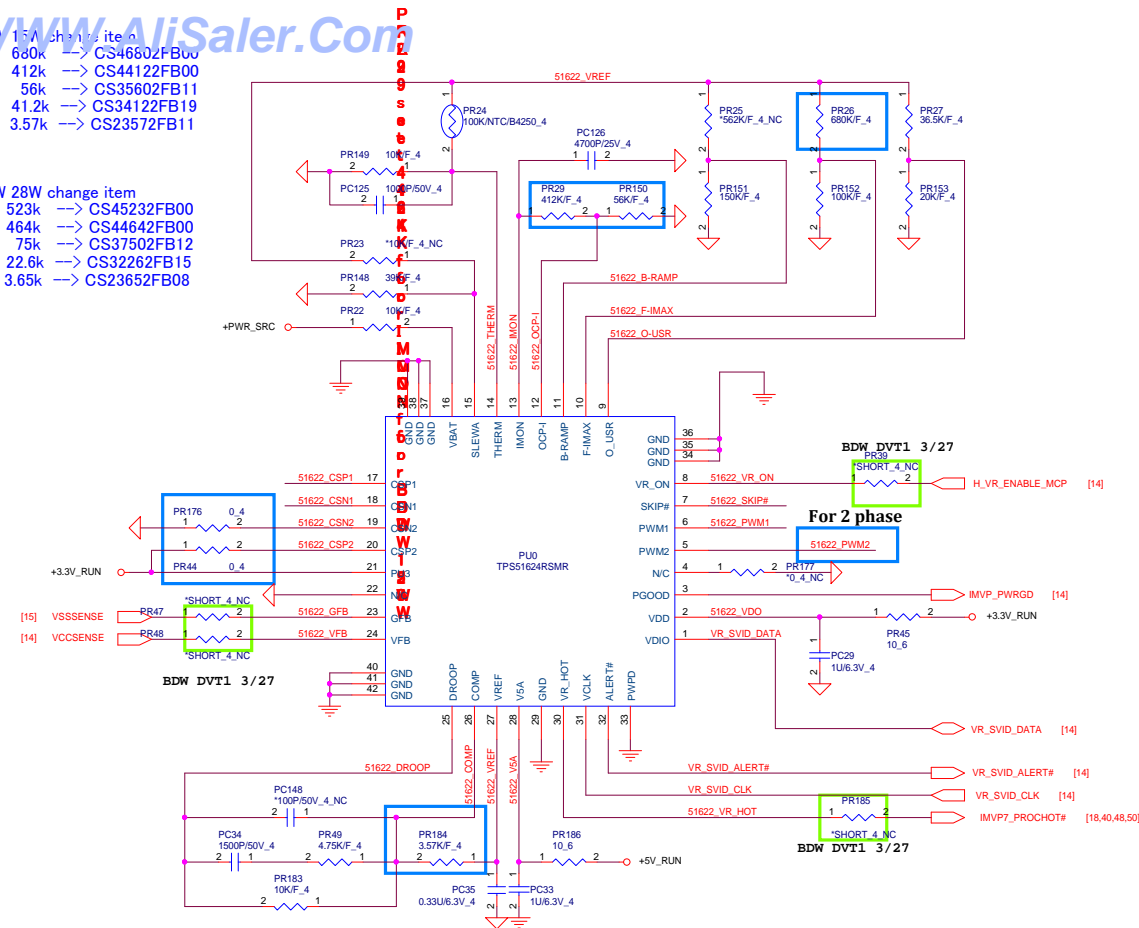


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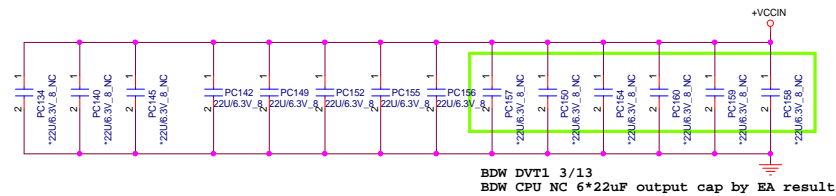
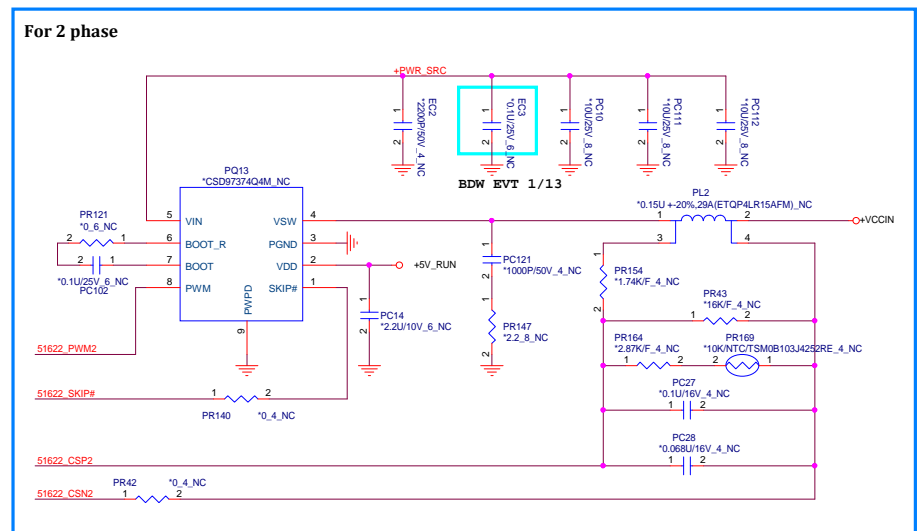
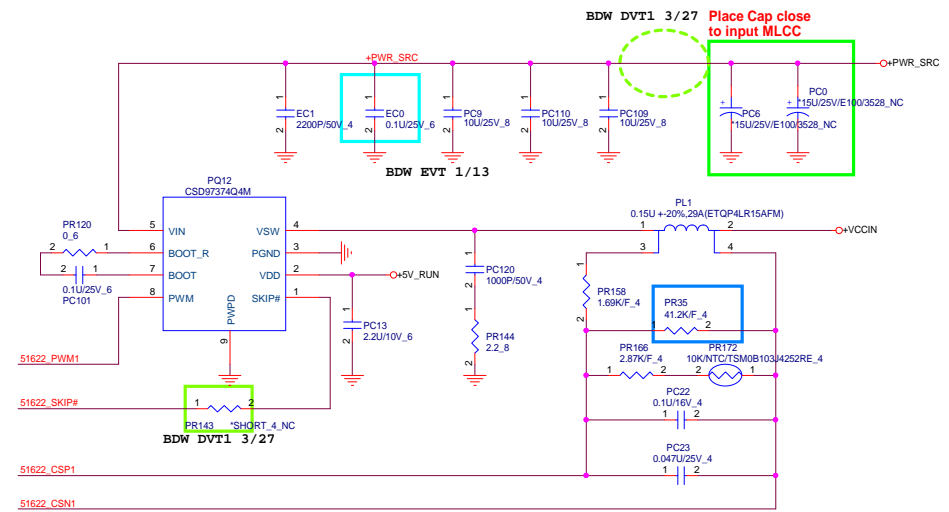
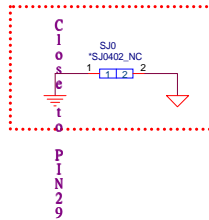
Size	Document Number	Rev
	+1.5V_RUN (G9661-25ADJF12U)	A
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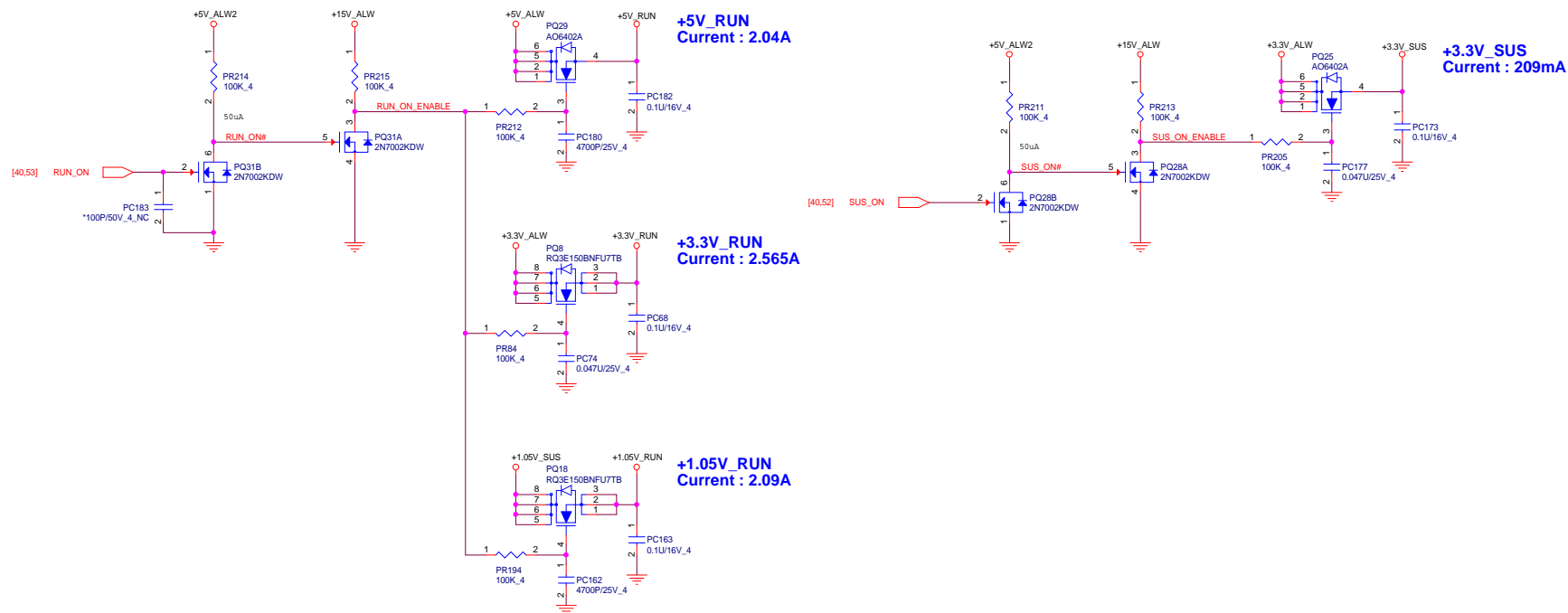
For BDW 28W change item

PR26	523k	→	CS45232FB00
PR29	464k	→	CS44642FB00
PR150	75k	→	CS37502FB12
PR35	22.6k	→	CS32262FB15
PR184	3.65k	→	CS23652FB08



For HSW 4	For BDW
IC1: TPS51622RSMR PN: AL051622001	IC1: TPS51624RSMR PN: AL051624000





+1.35V_GFX Volt +/- 5%
TDC: 2.585A
Peak: 4A
OCP: 6A

Boot VID voltage is 0.9V
 Set OFSA to 1.65V
 $+1.35V_GFX = (1.65 - 1.2) + 0.9 = 1.35V$

+1.05V_GFX
Current : 1.33A

+3V_GFX
Current : 22mA

BDW DVT1 3/31, confirmed with EE
 Add +1.8V_GFX discharge circuit

BDW EVT 1/13, confirmed with EE
 Add +3V_GFX discharge circuit

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